

GA102 GF SKU P-BOARD

350W, 384bit, GDDR6x x8 24GB

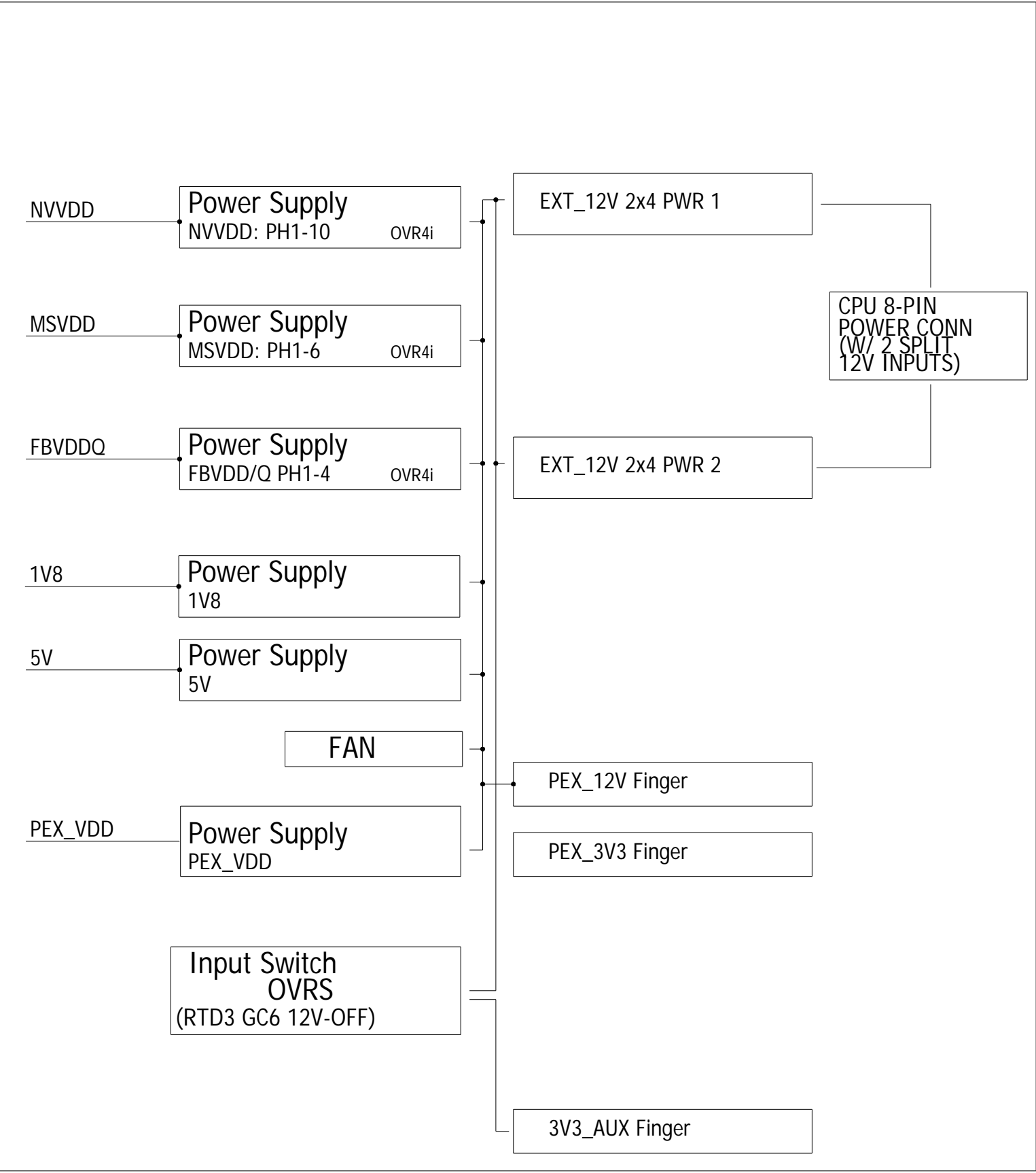
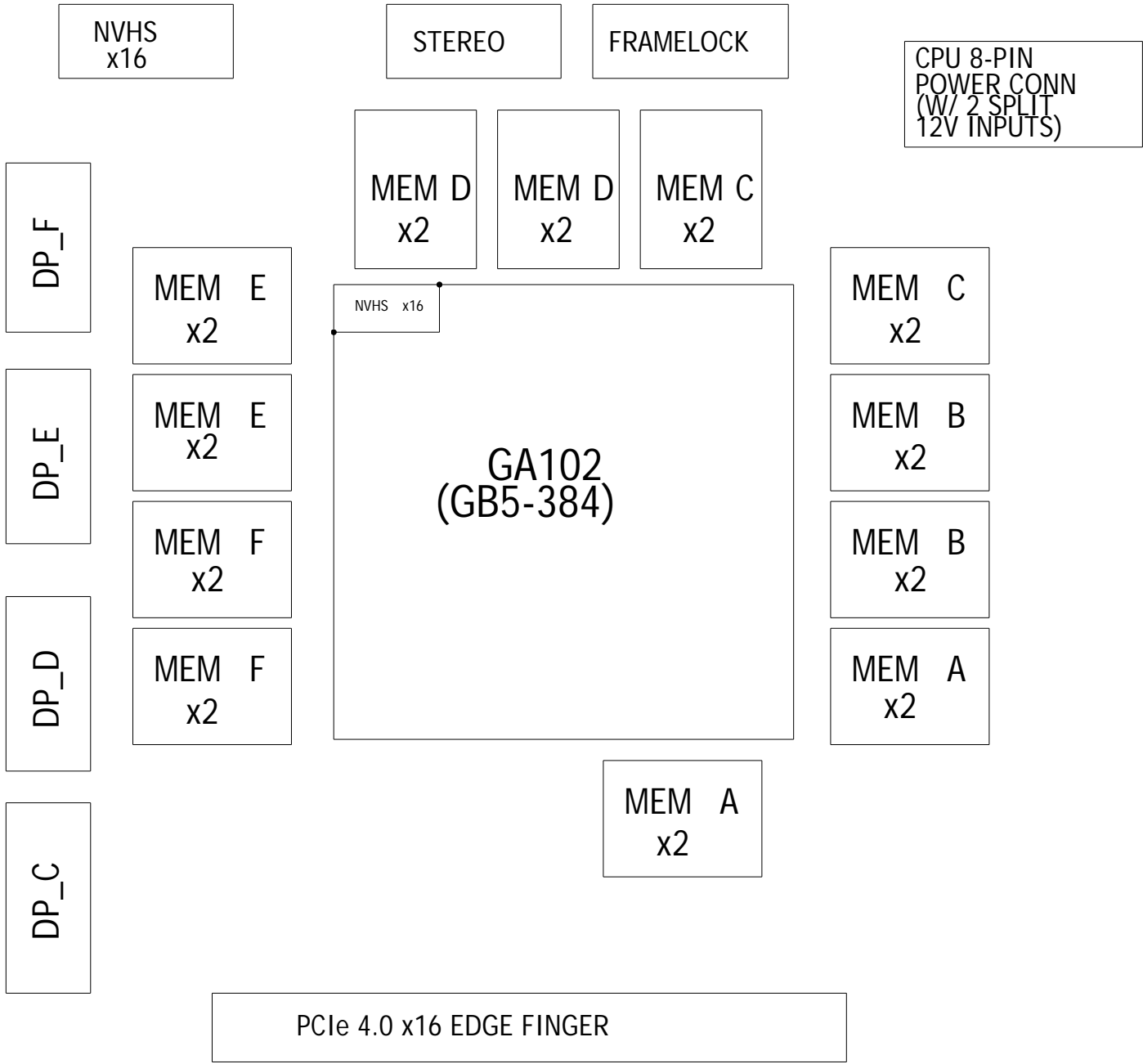
DP + DP + DP + HDMI

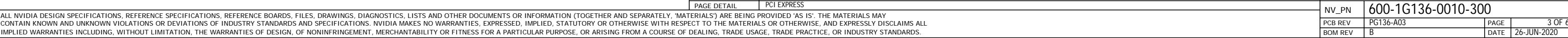
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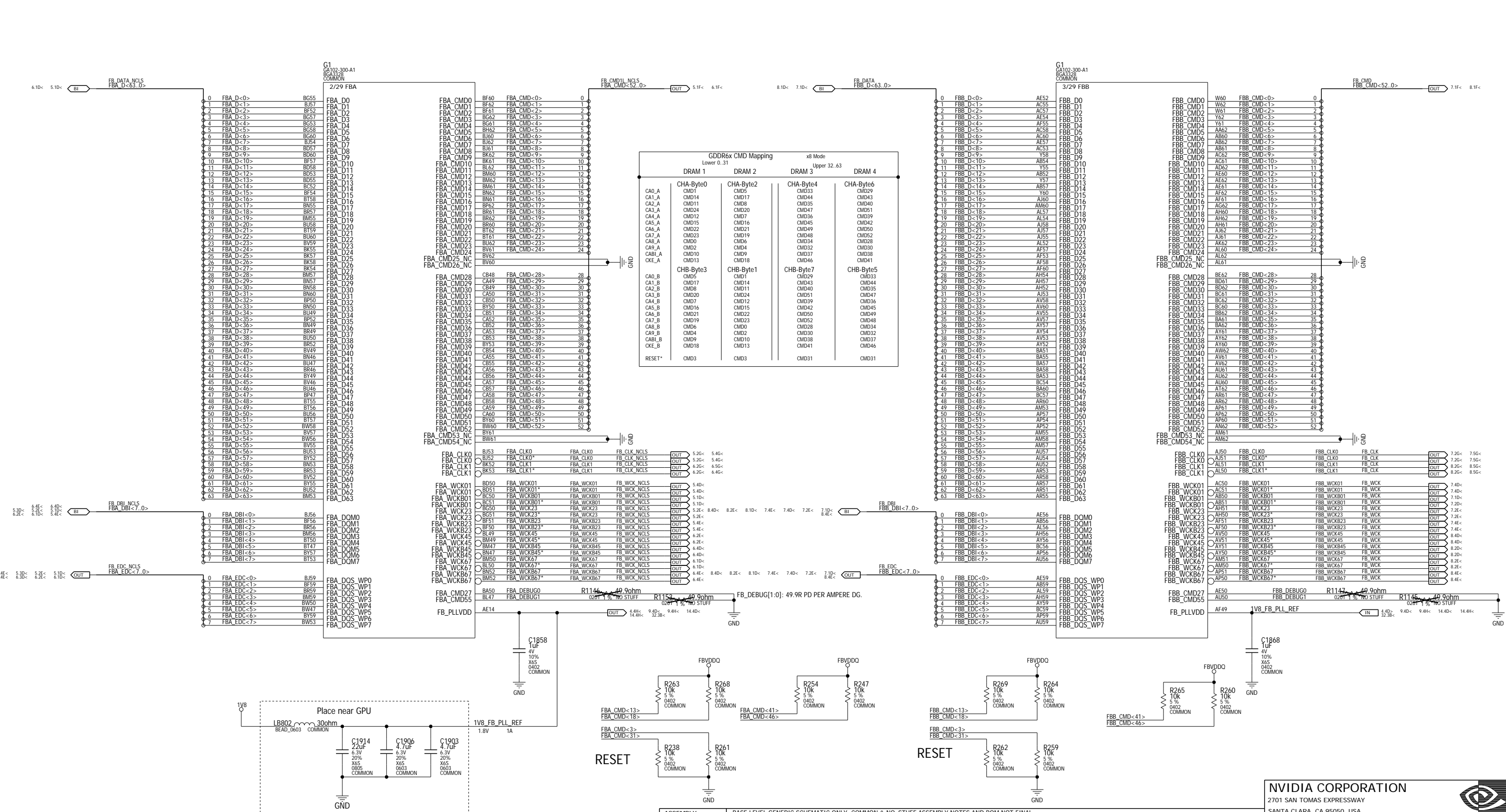
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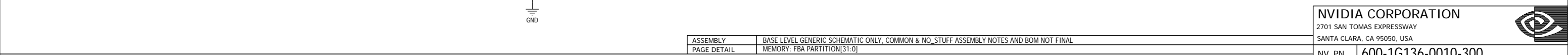
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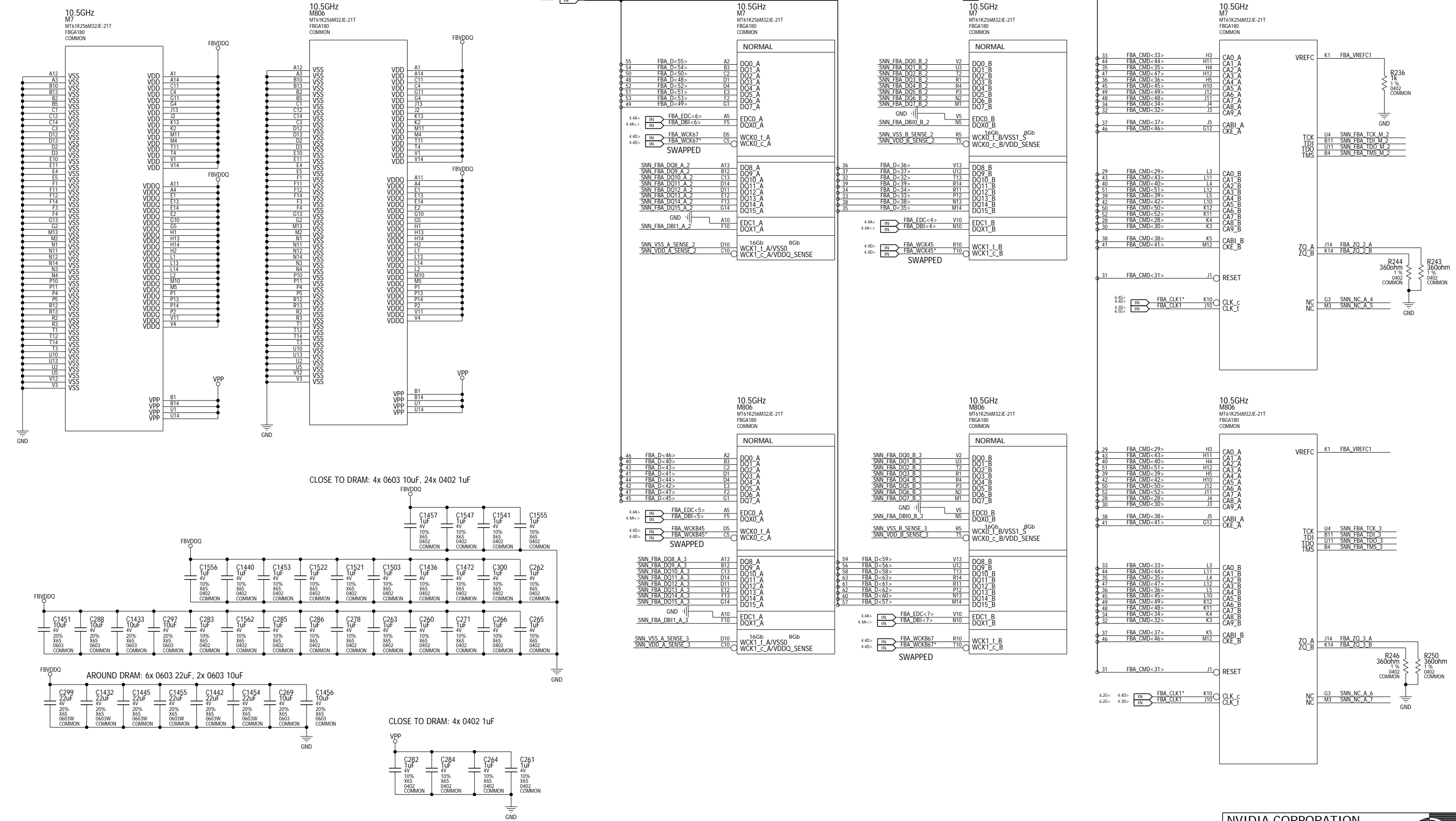
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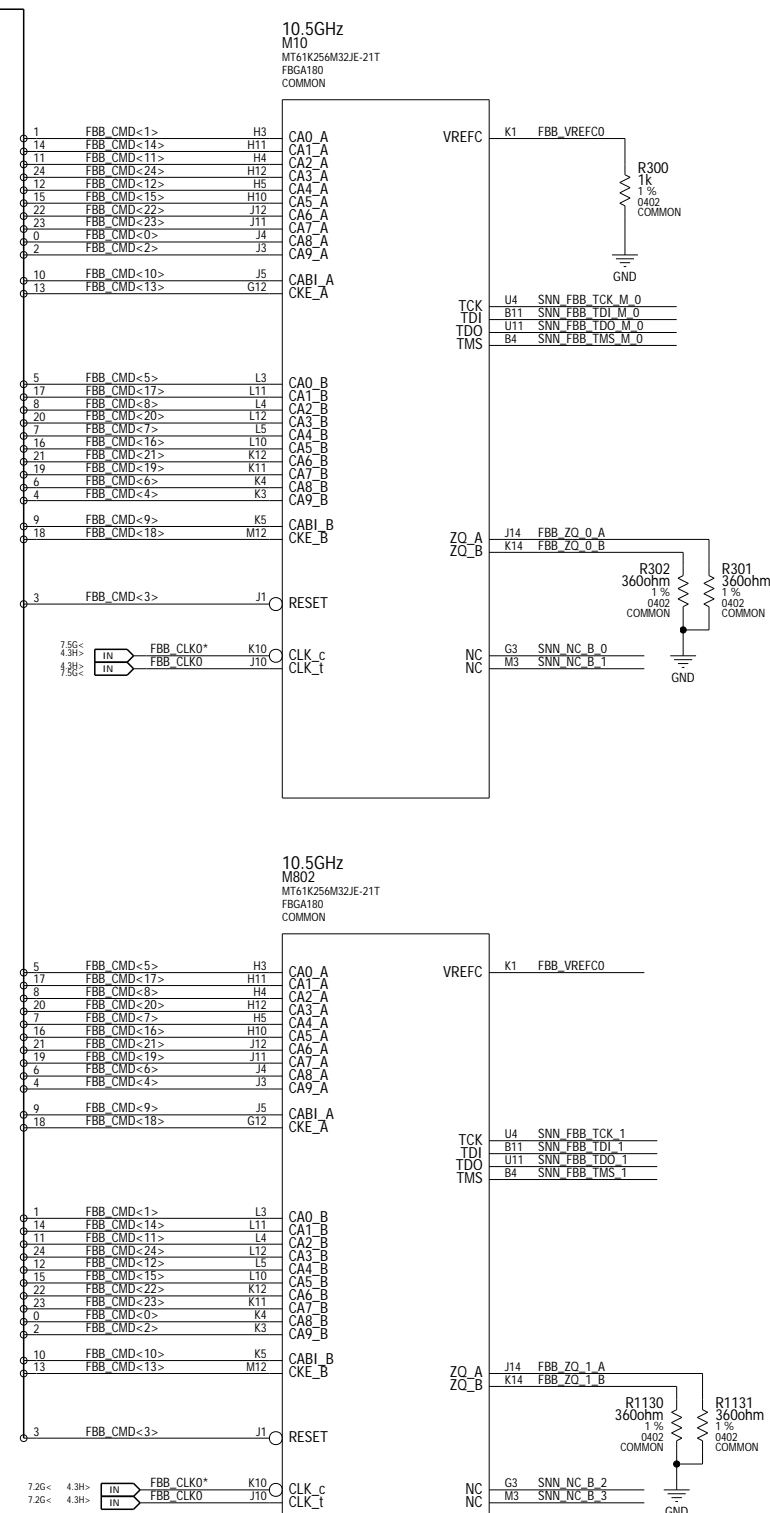
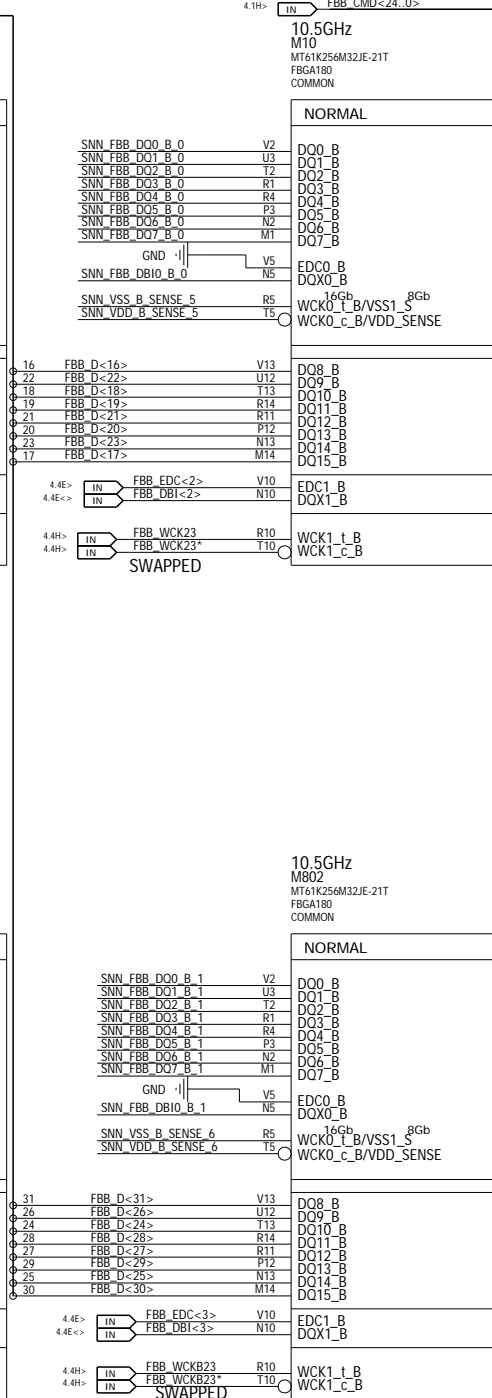
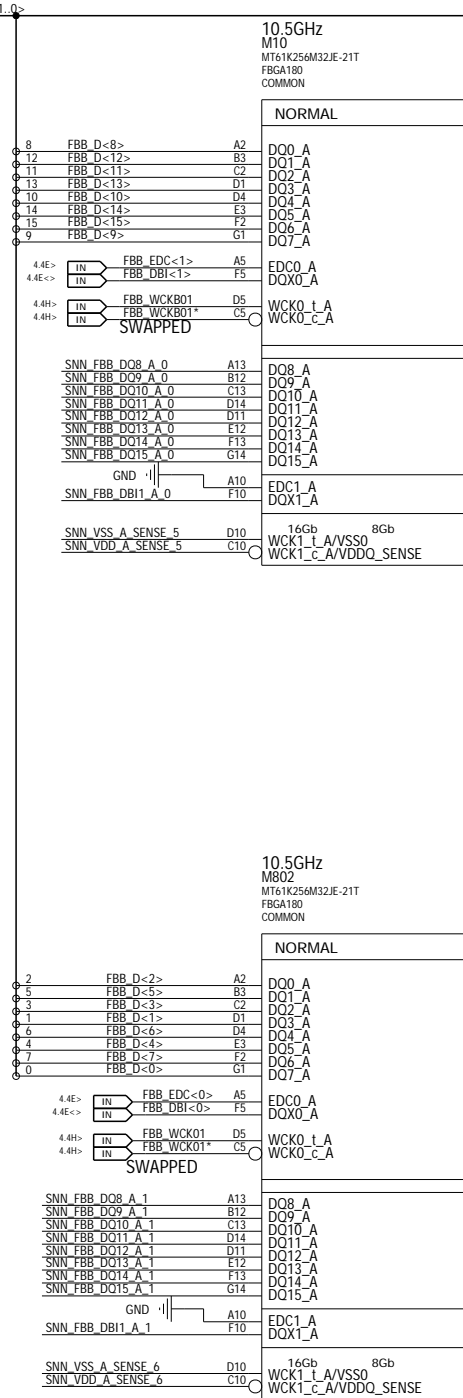
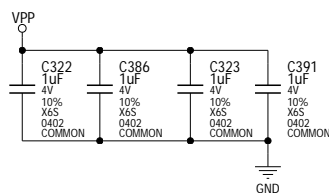
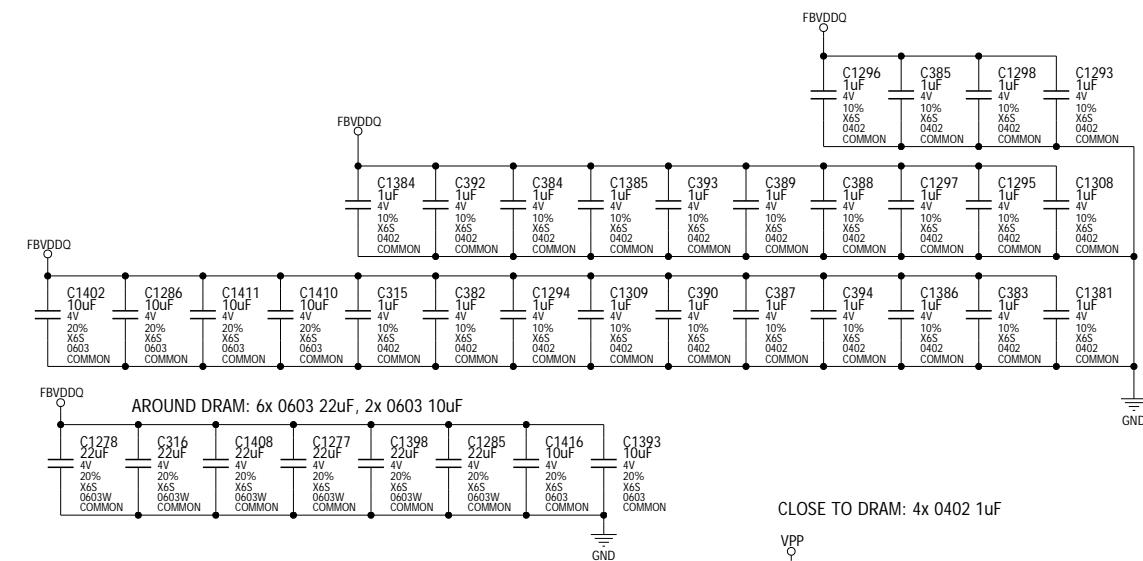
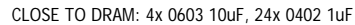
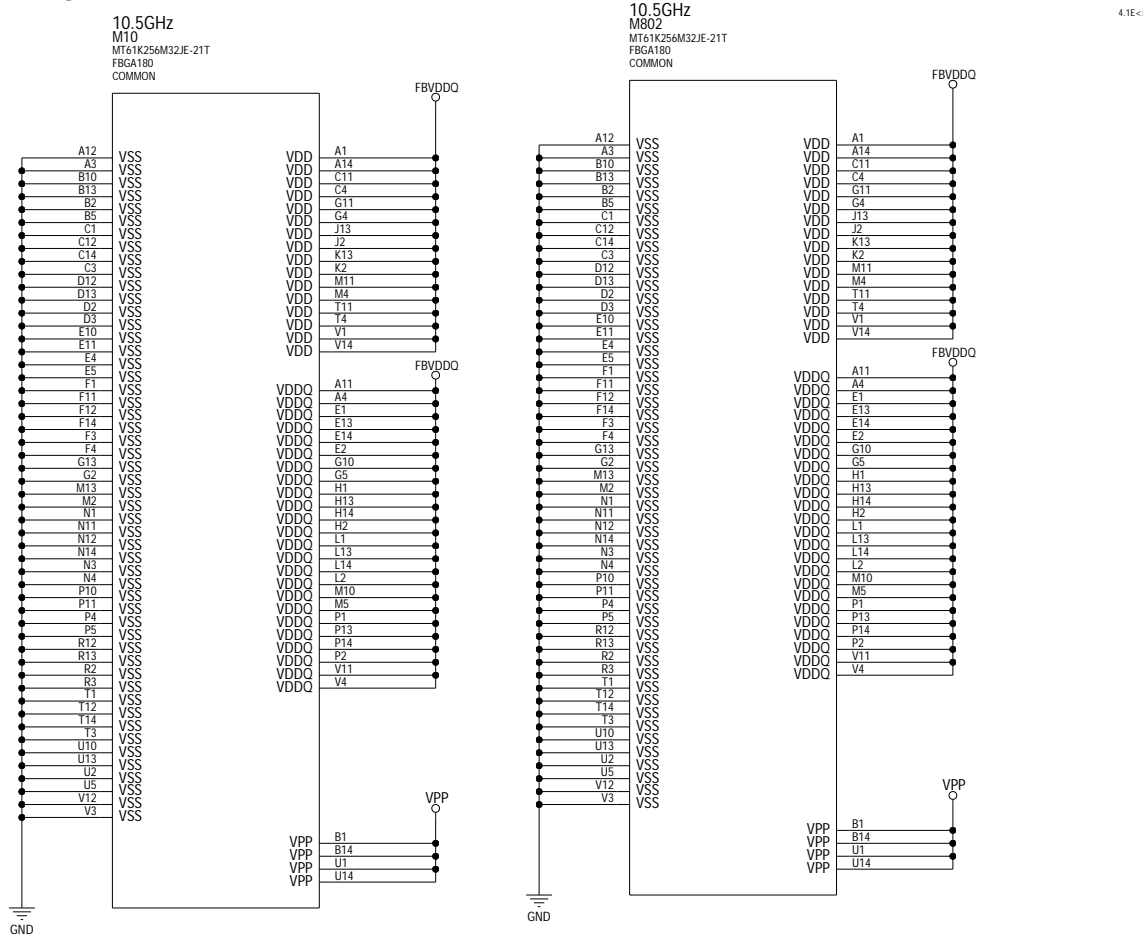








Page7: MEMORY: FBB Partition 31..0



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PCB REV

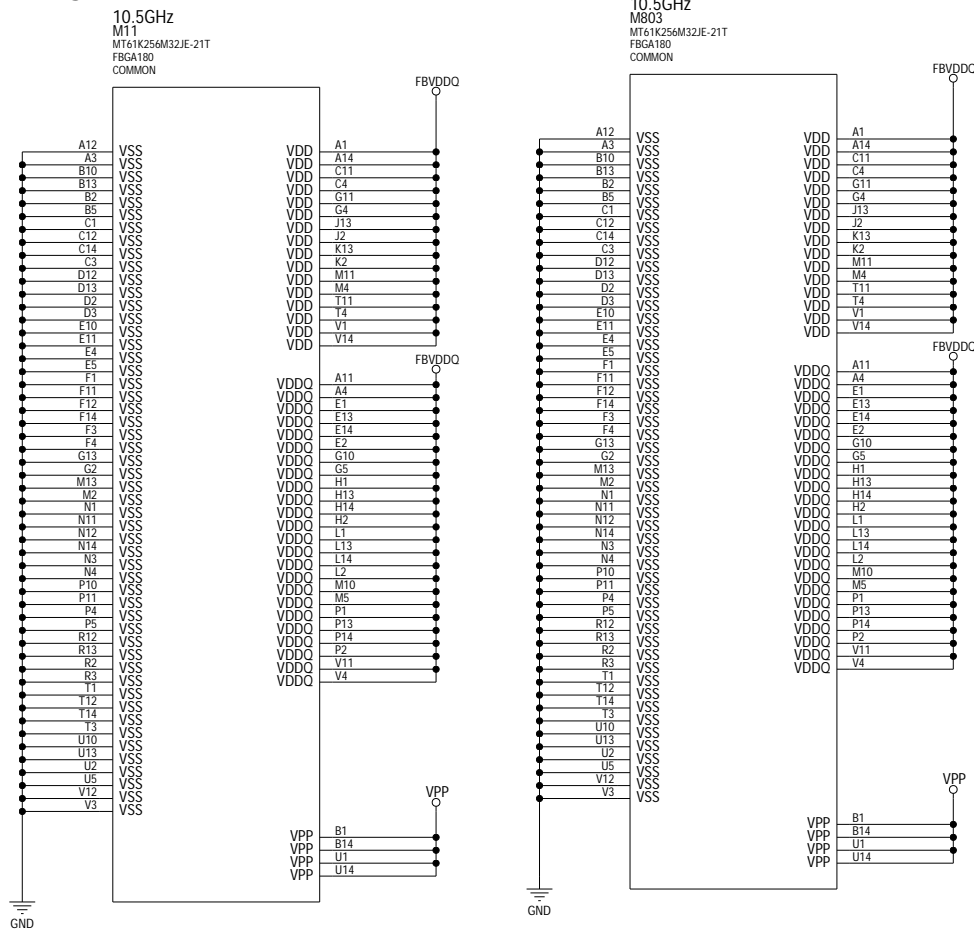
PG136-A03

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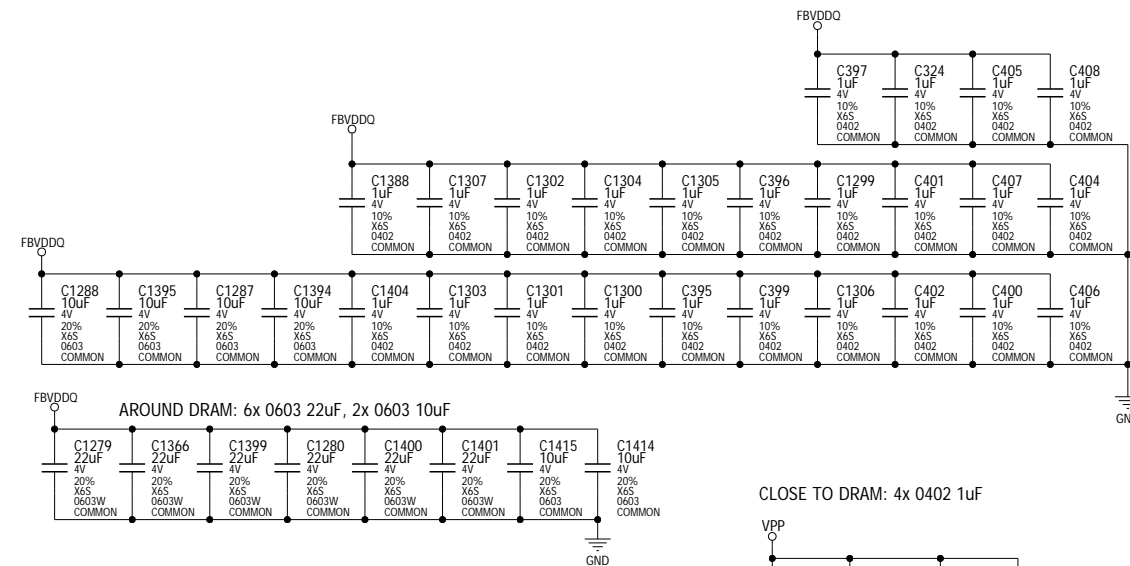
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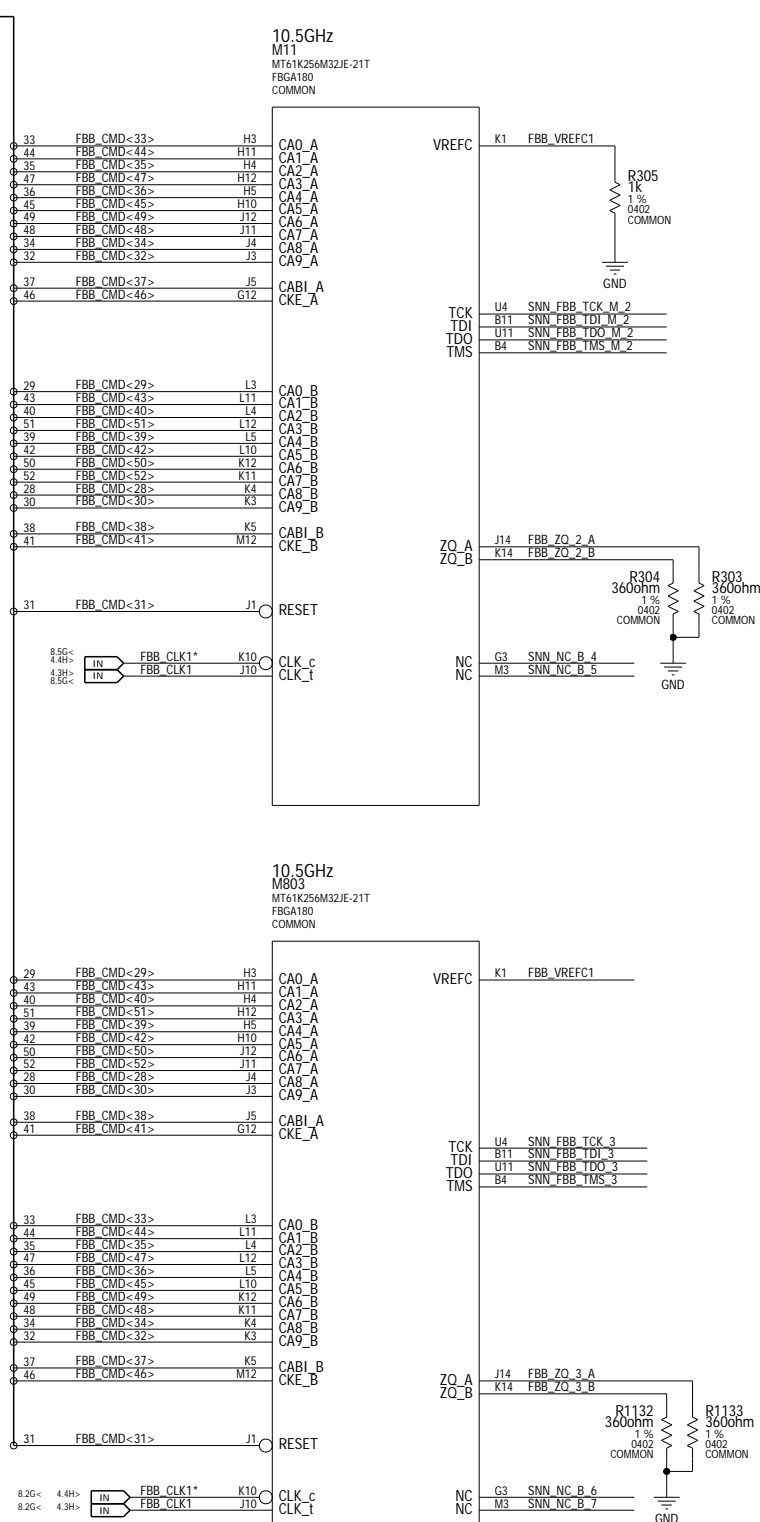
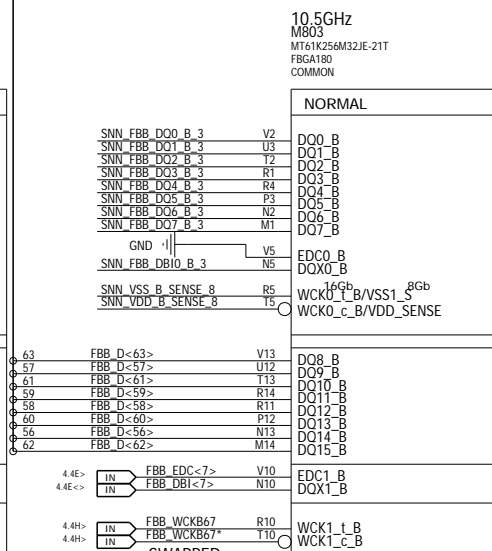
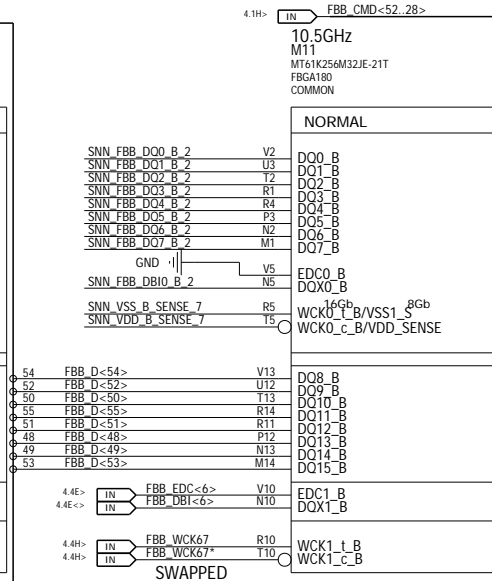
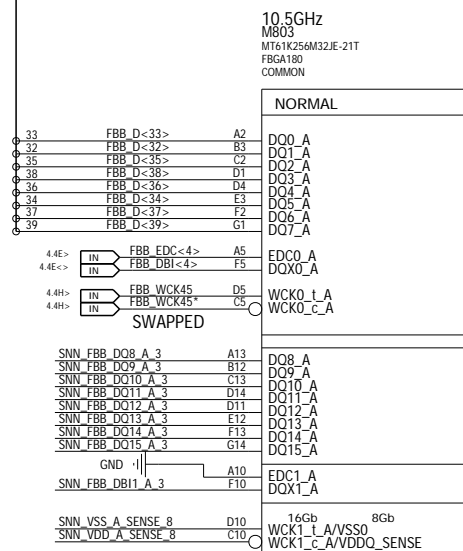
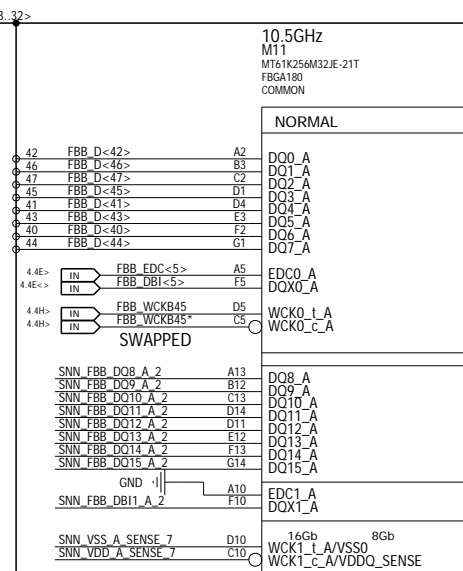
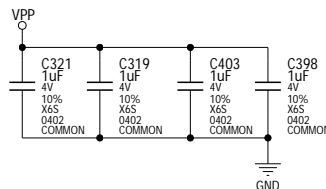
Page8: MEMORY: FBB Partition 63..32

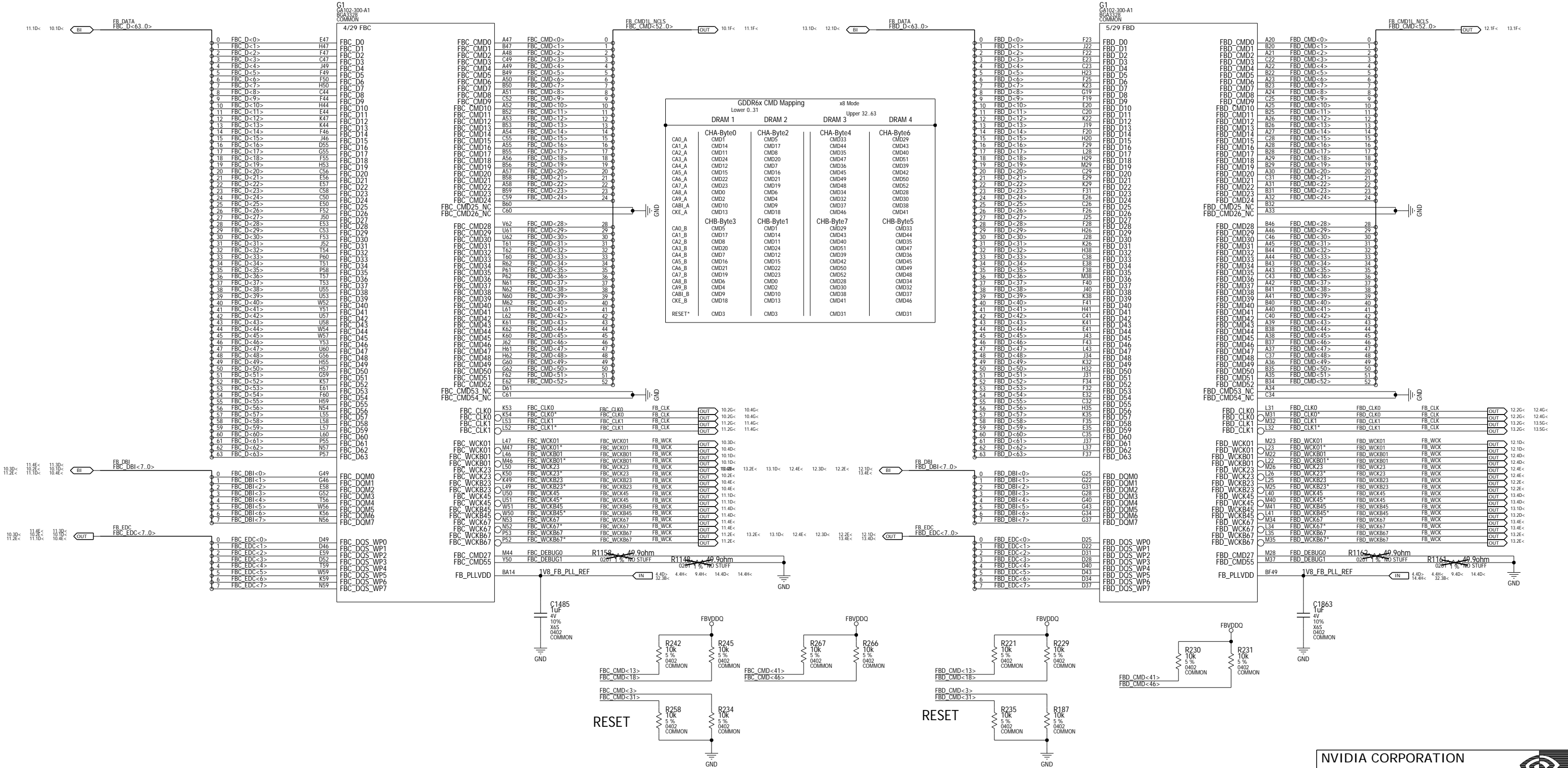


CLOSE TO DRAM: 4x 0603 10uF, 24x 0402 1uF

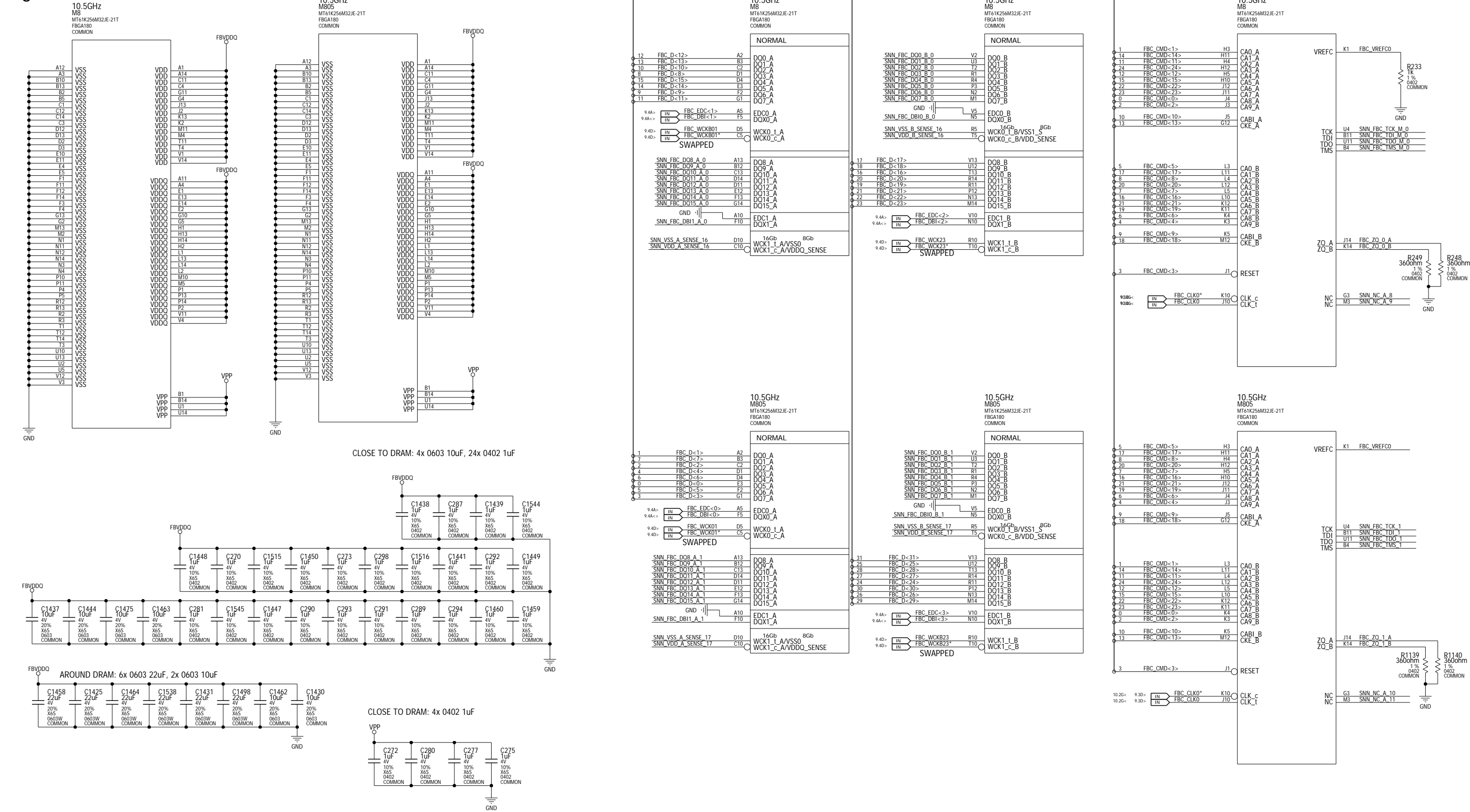


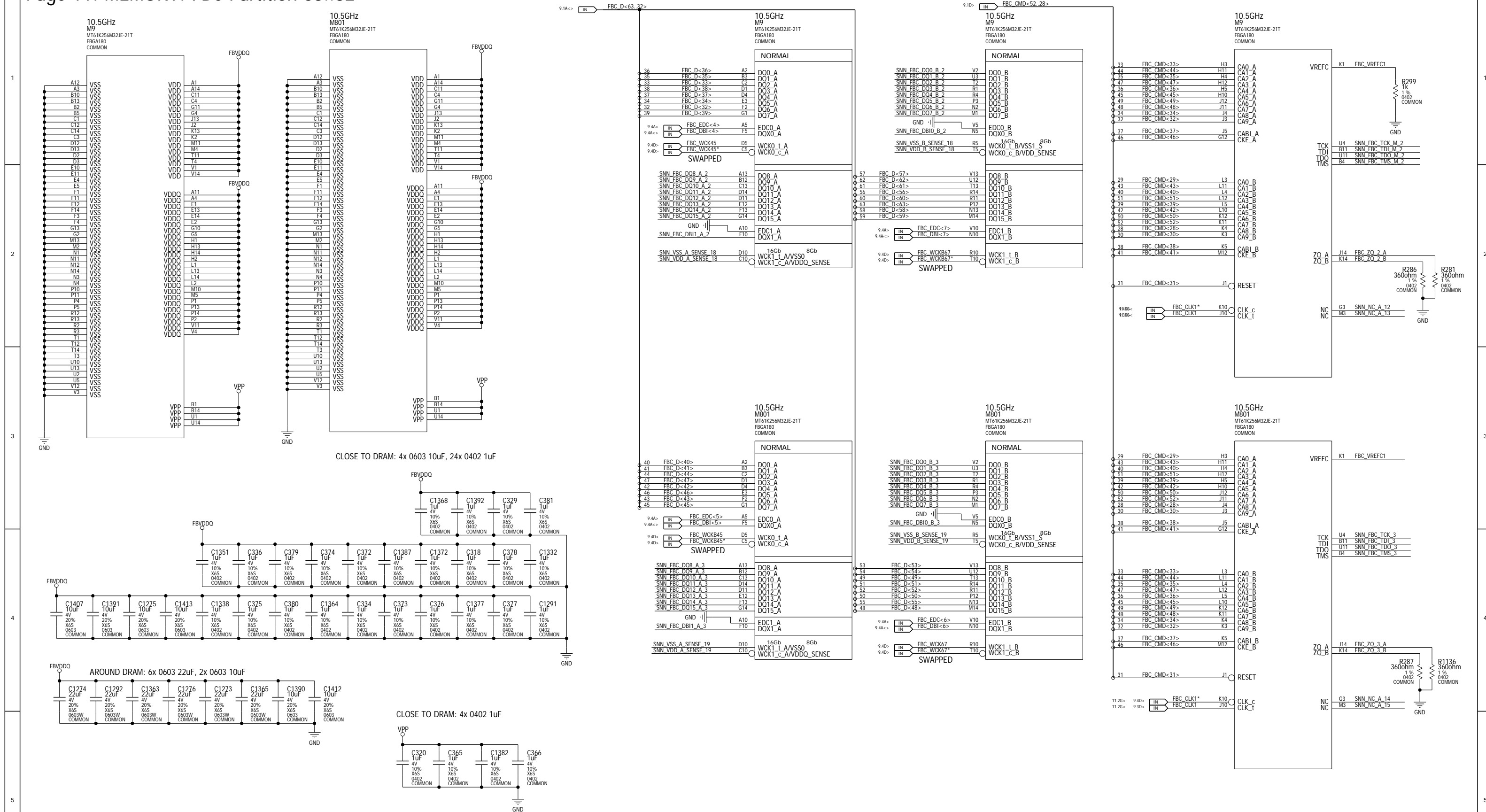
CLOSE TO DRAM: 4x 0402 1uF

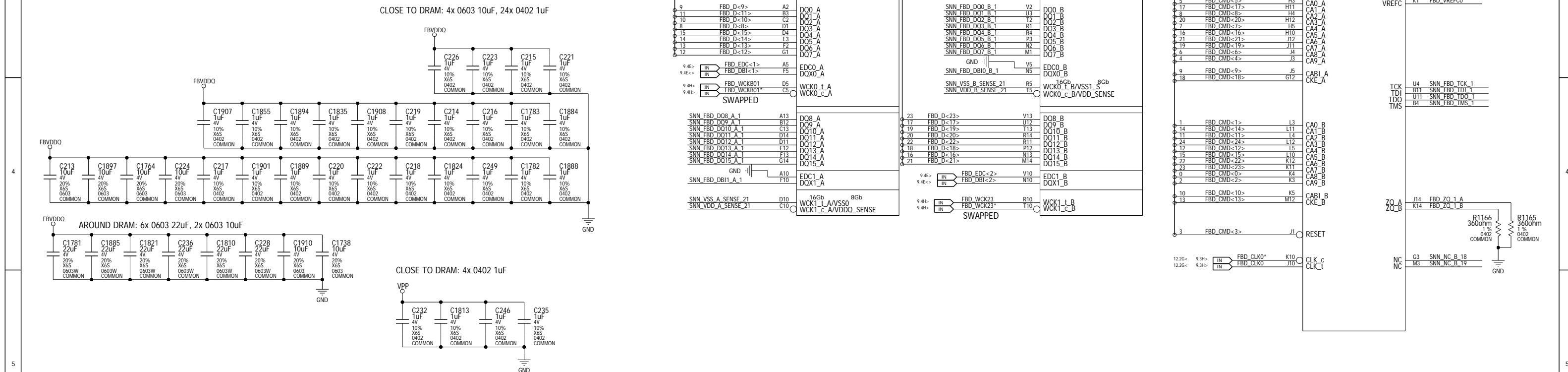
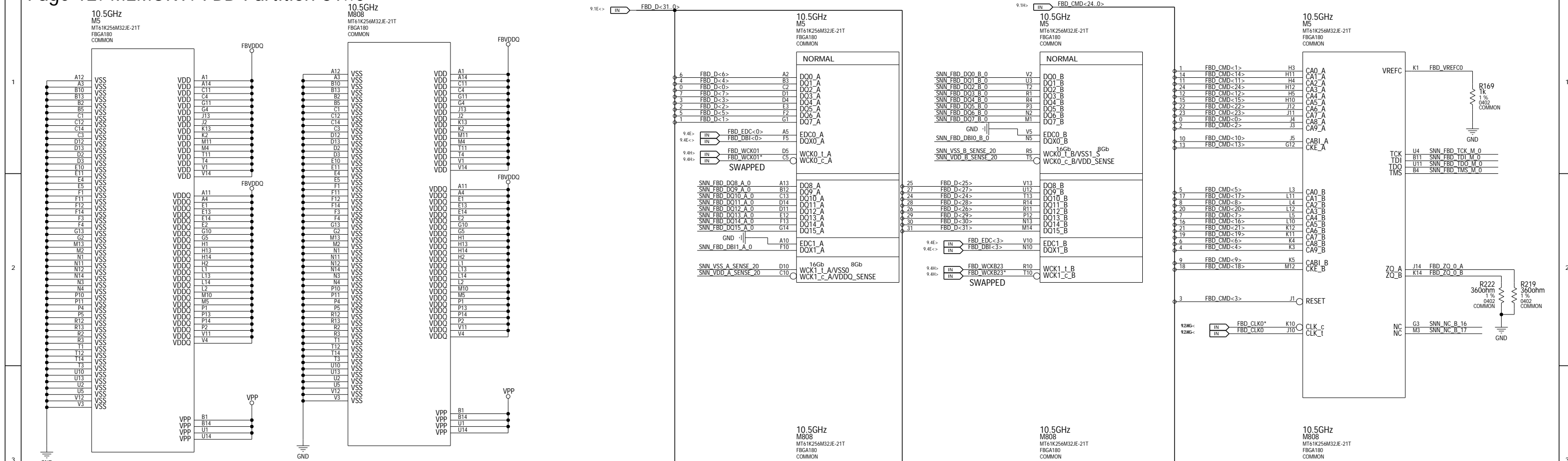


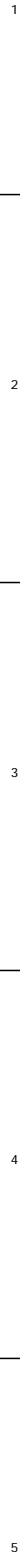


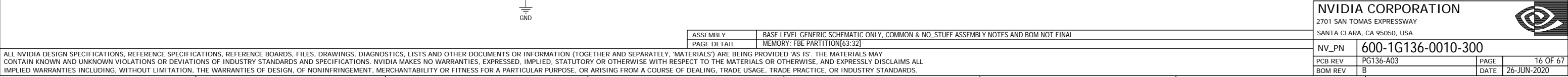
Page 10: MEMORY: FBC Partition 31..0



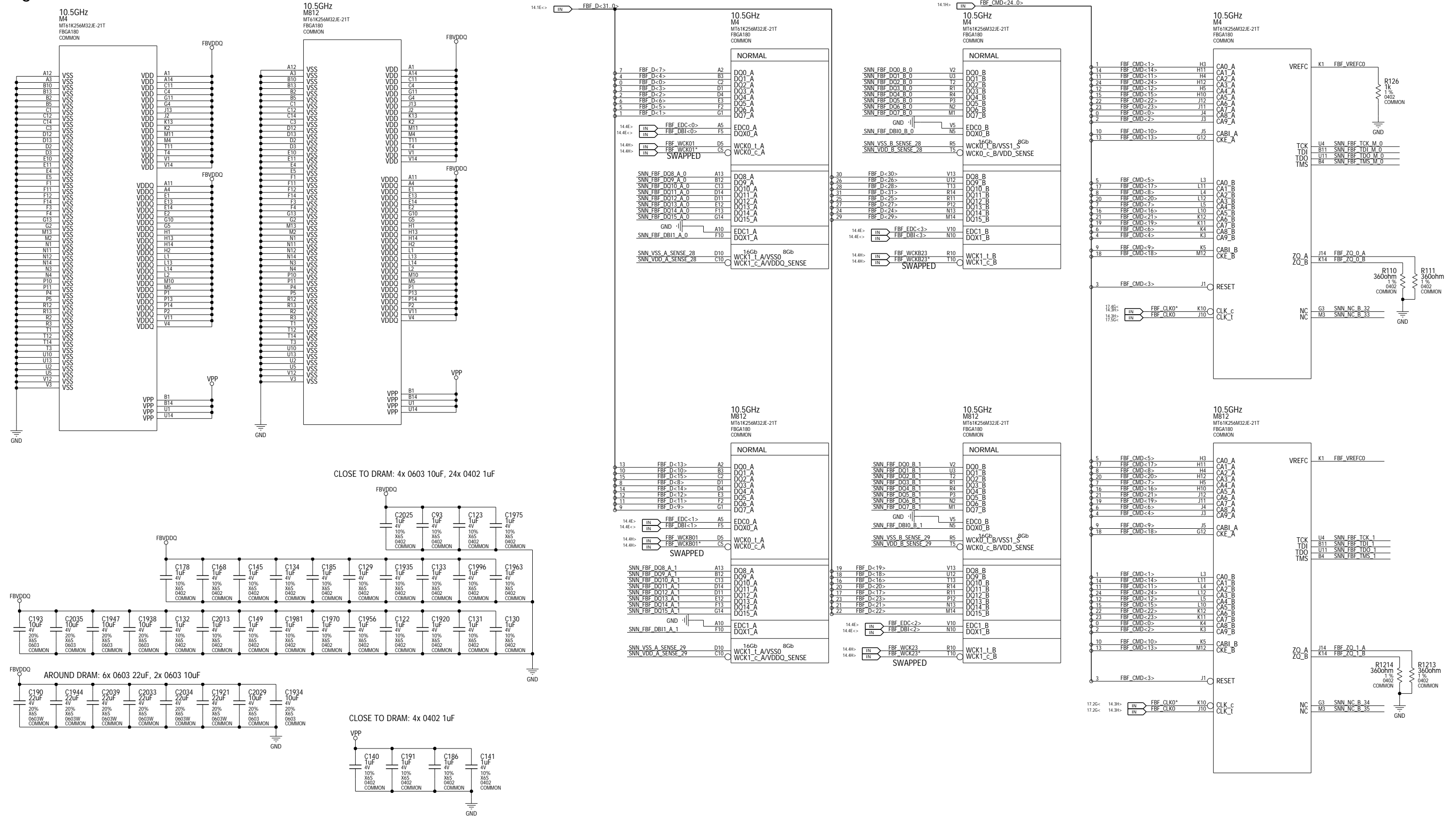


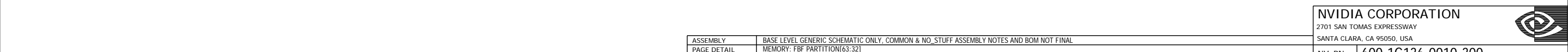


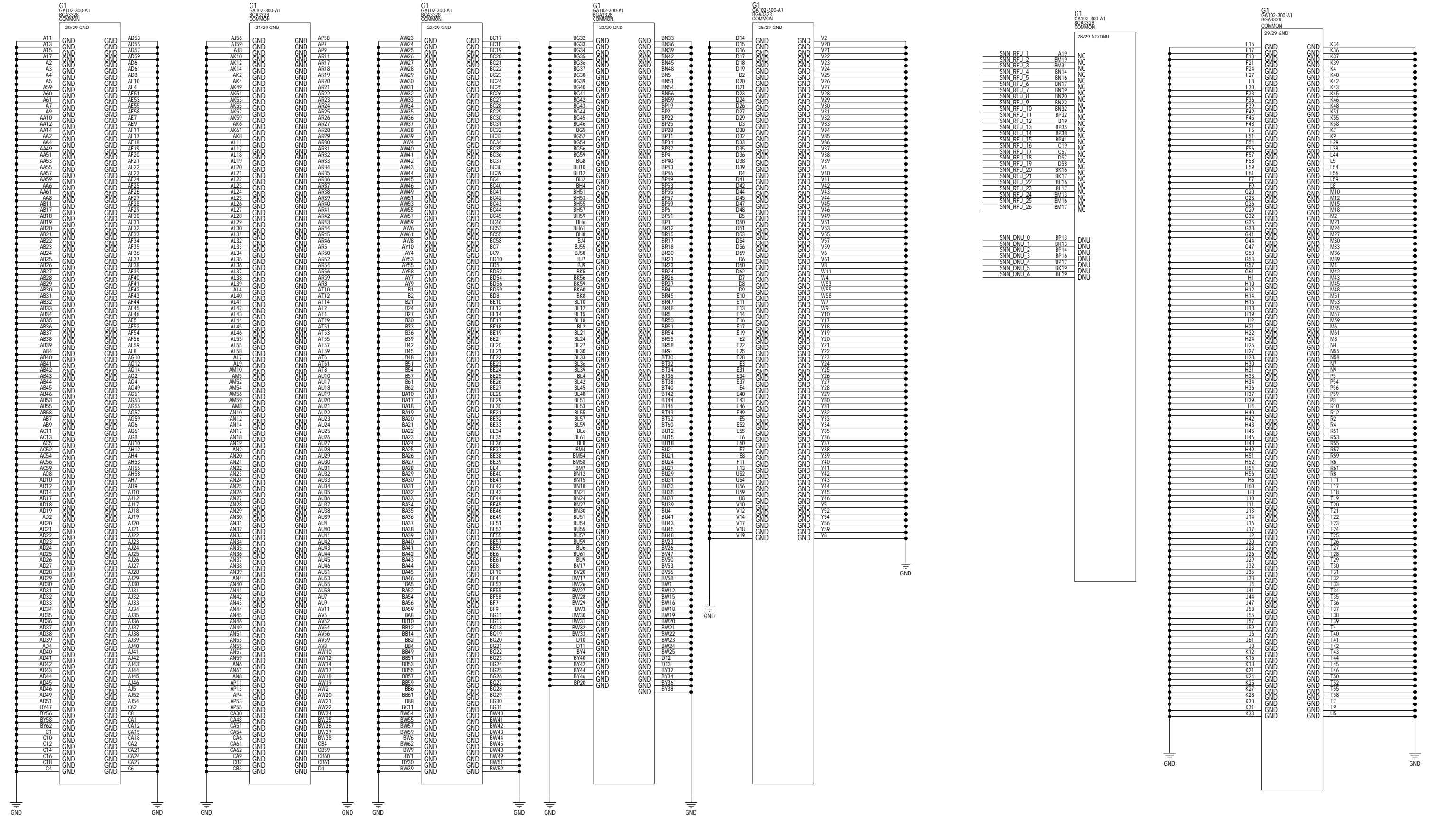


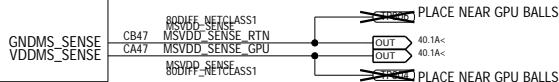
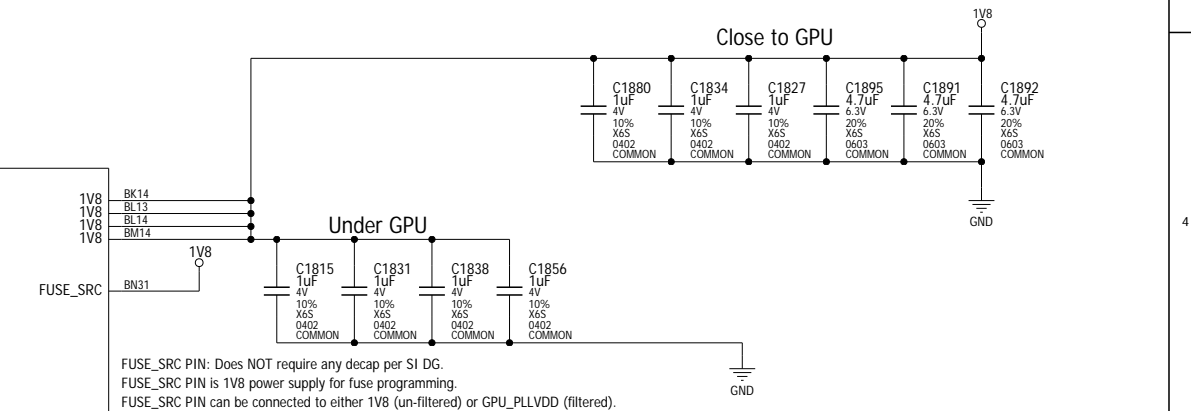
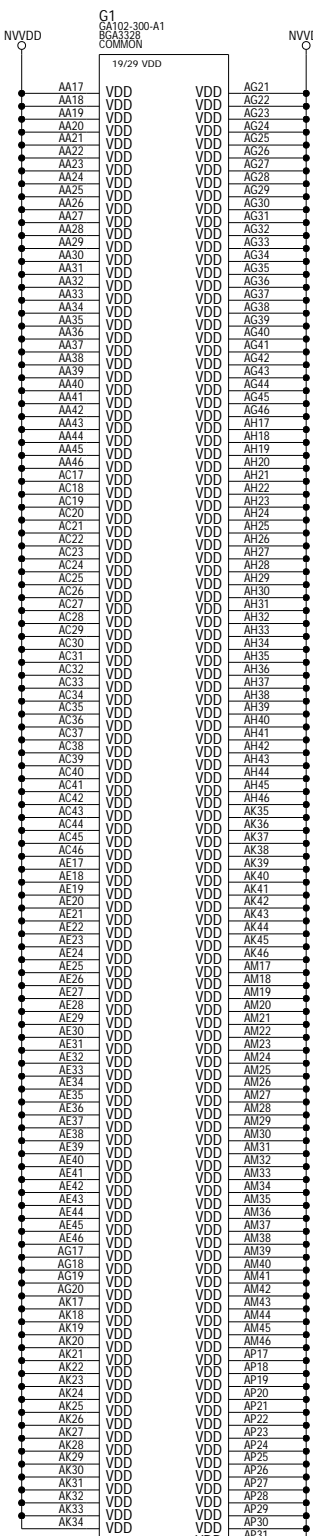



Page 17: MEMORY: FBF Partition 31..0





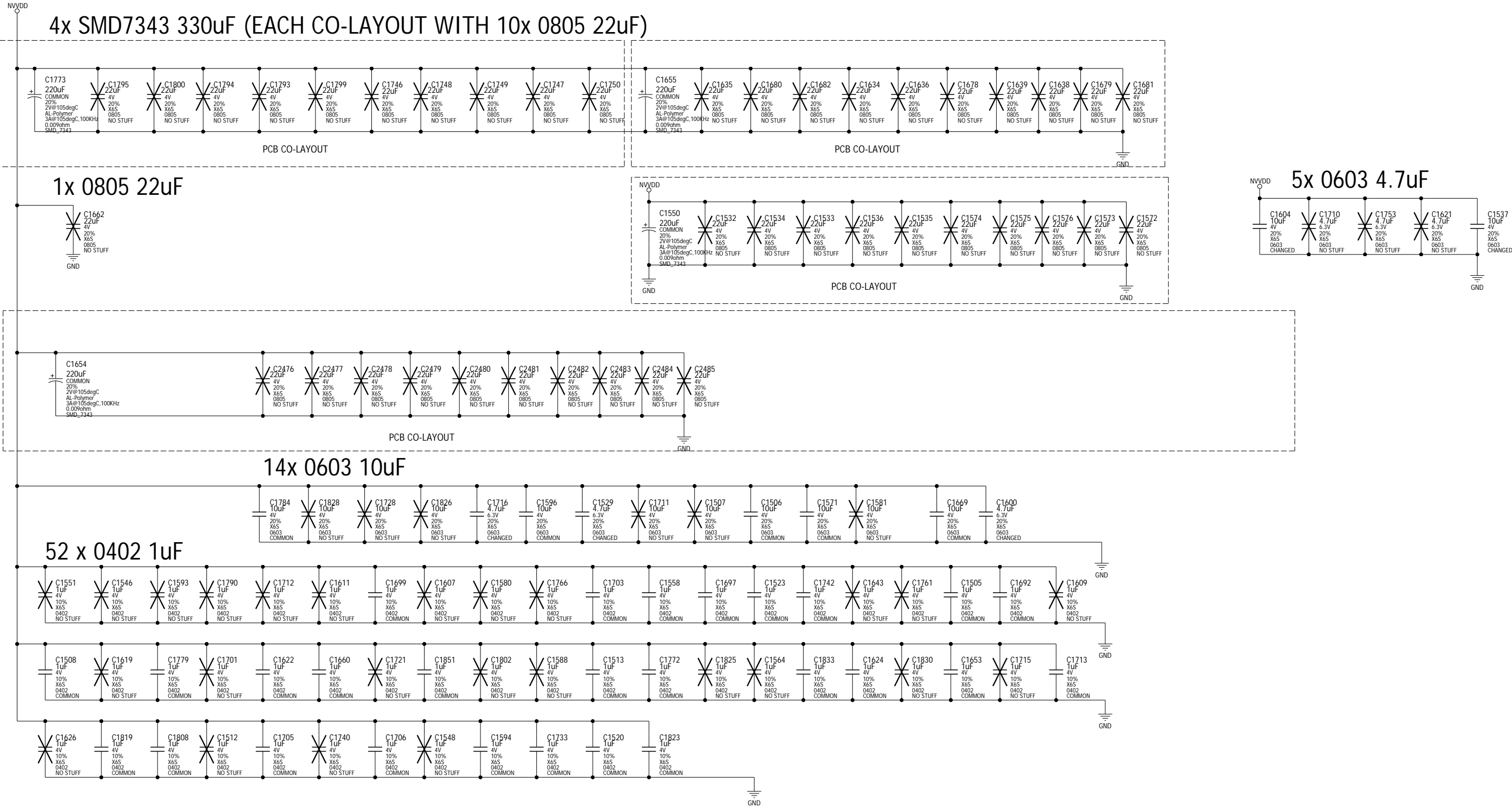




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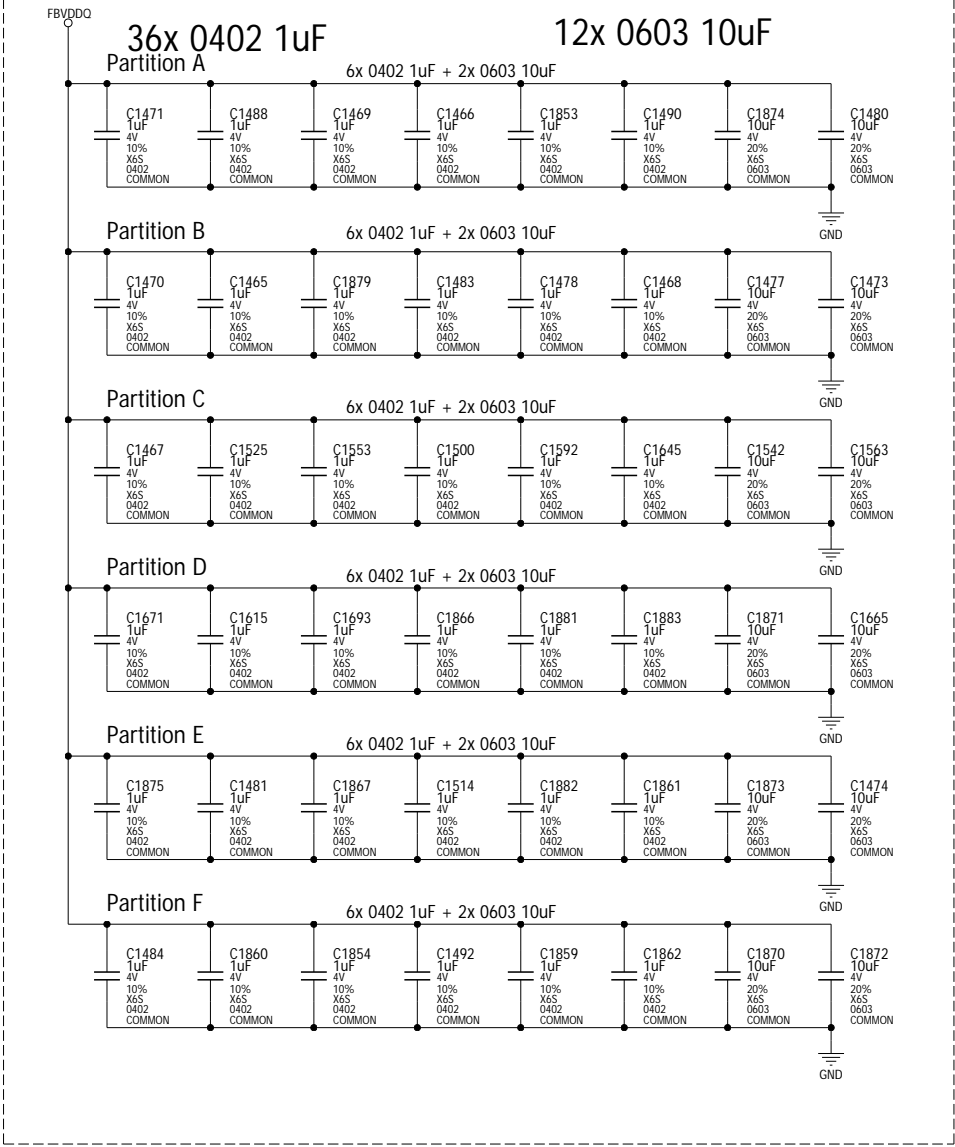
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NVVDD UNDER GPU

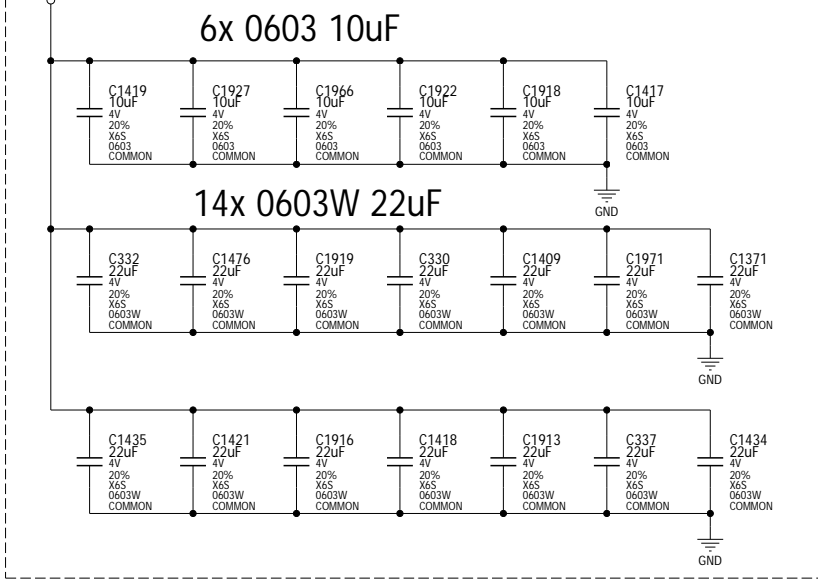


FBVDDQ

Under GPU



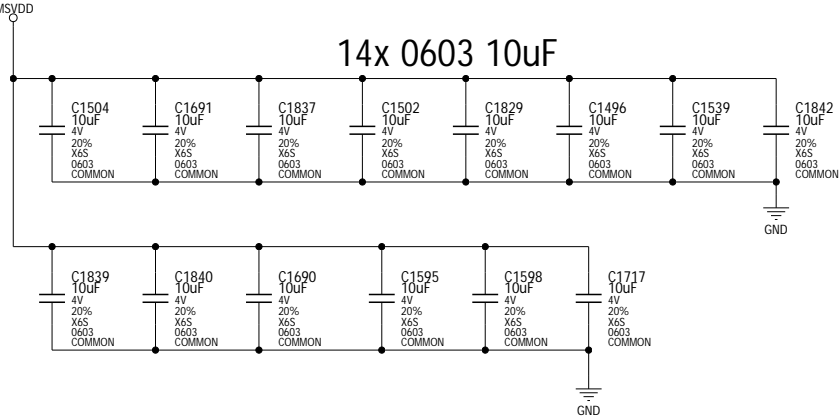
Close to GPU



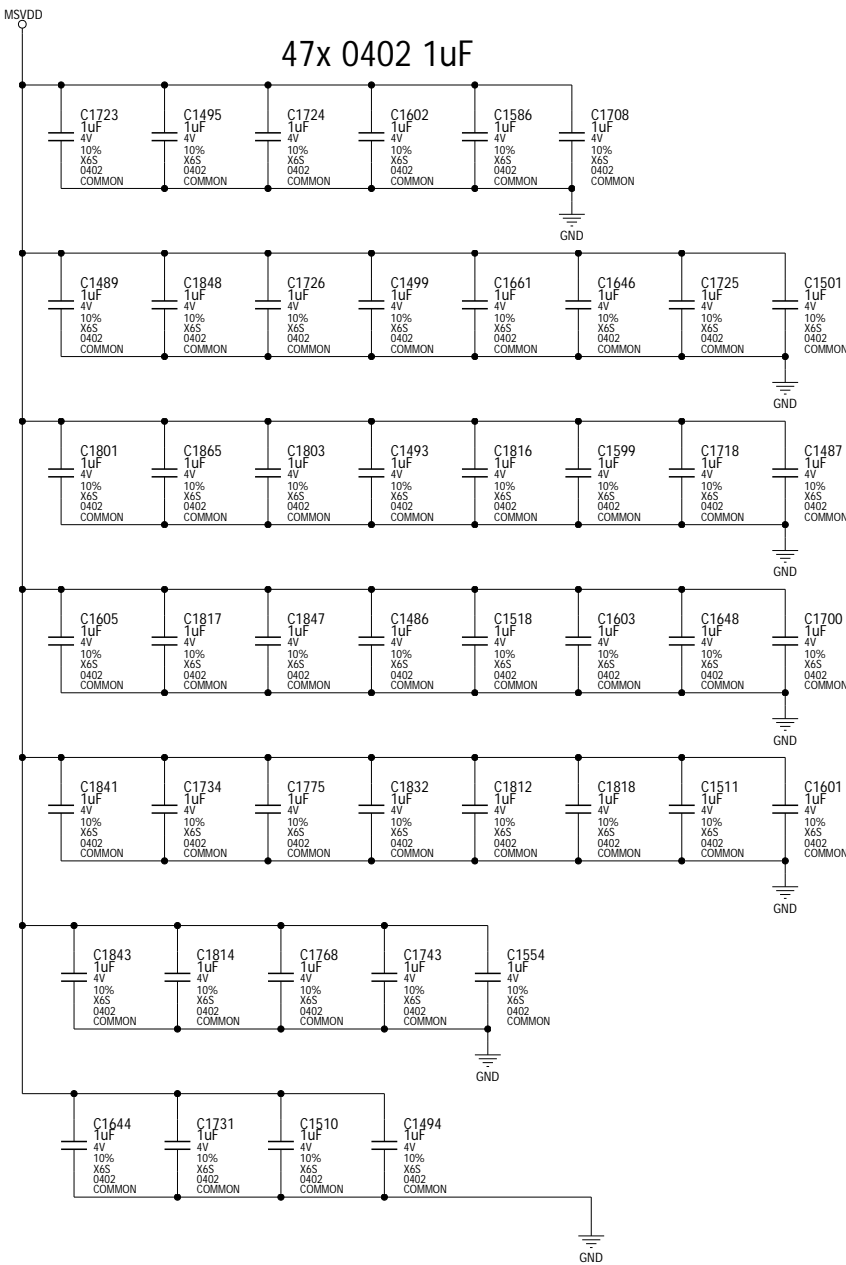
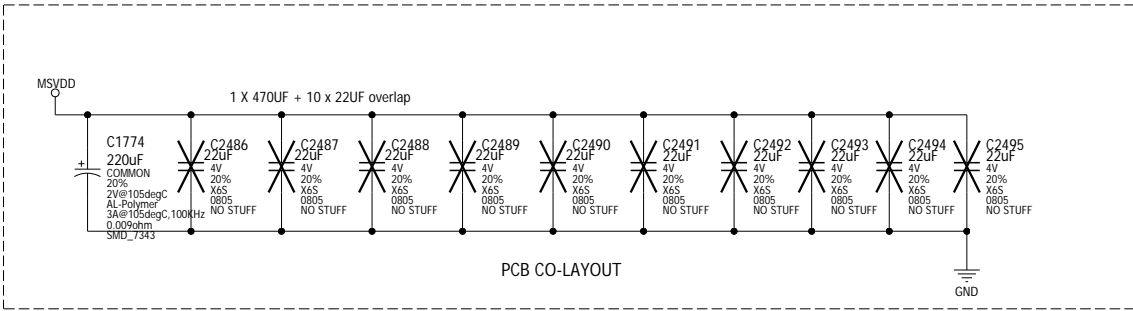
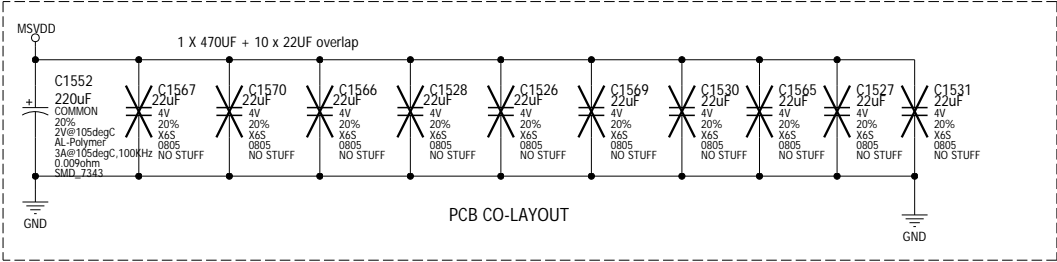
Page 23: GPU: MSVDD DECOUPLING

MSVDD

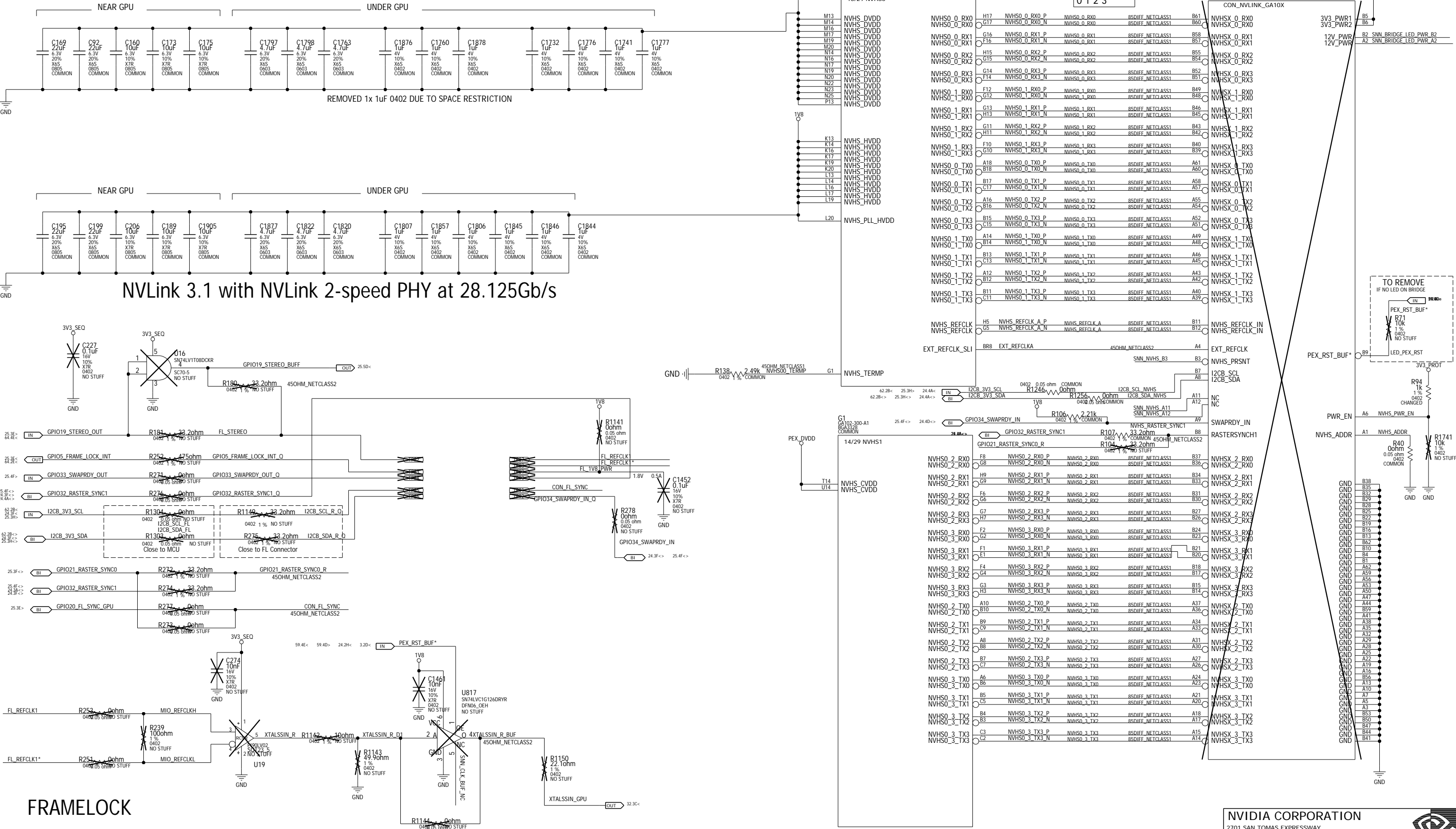
UNDER GPU



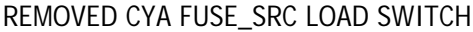
2x SMD7343 330uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



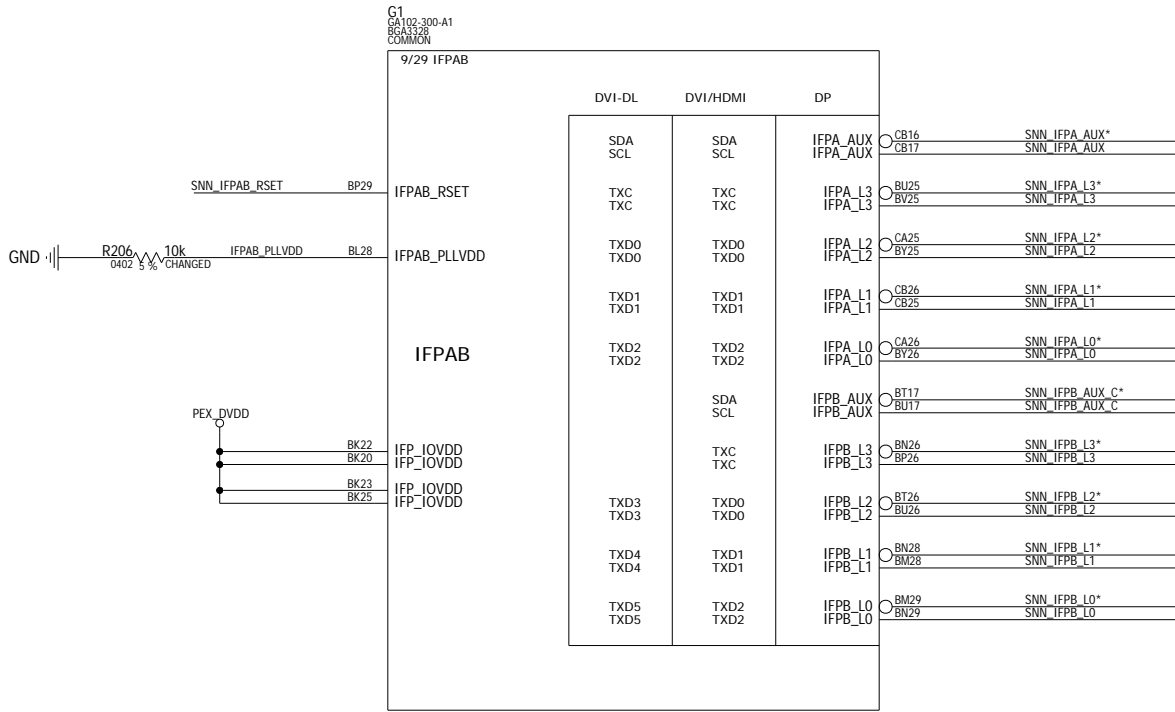
REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

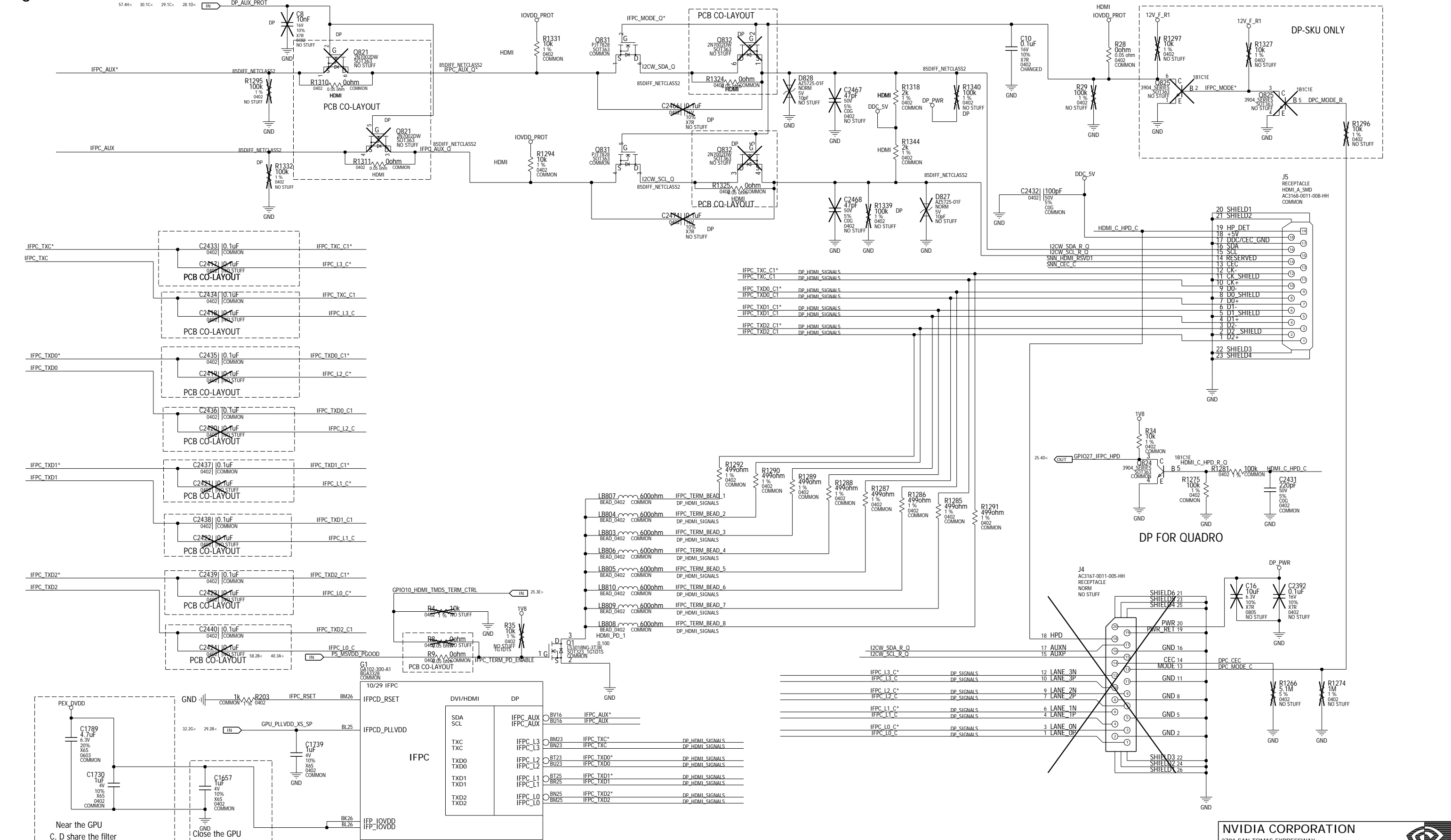


FRAMELOCK



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1

2

3

4

5

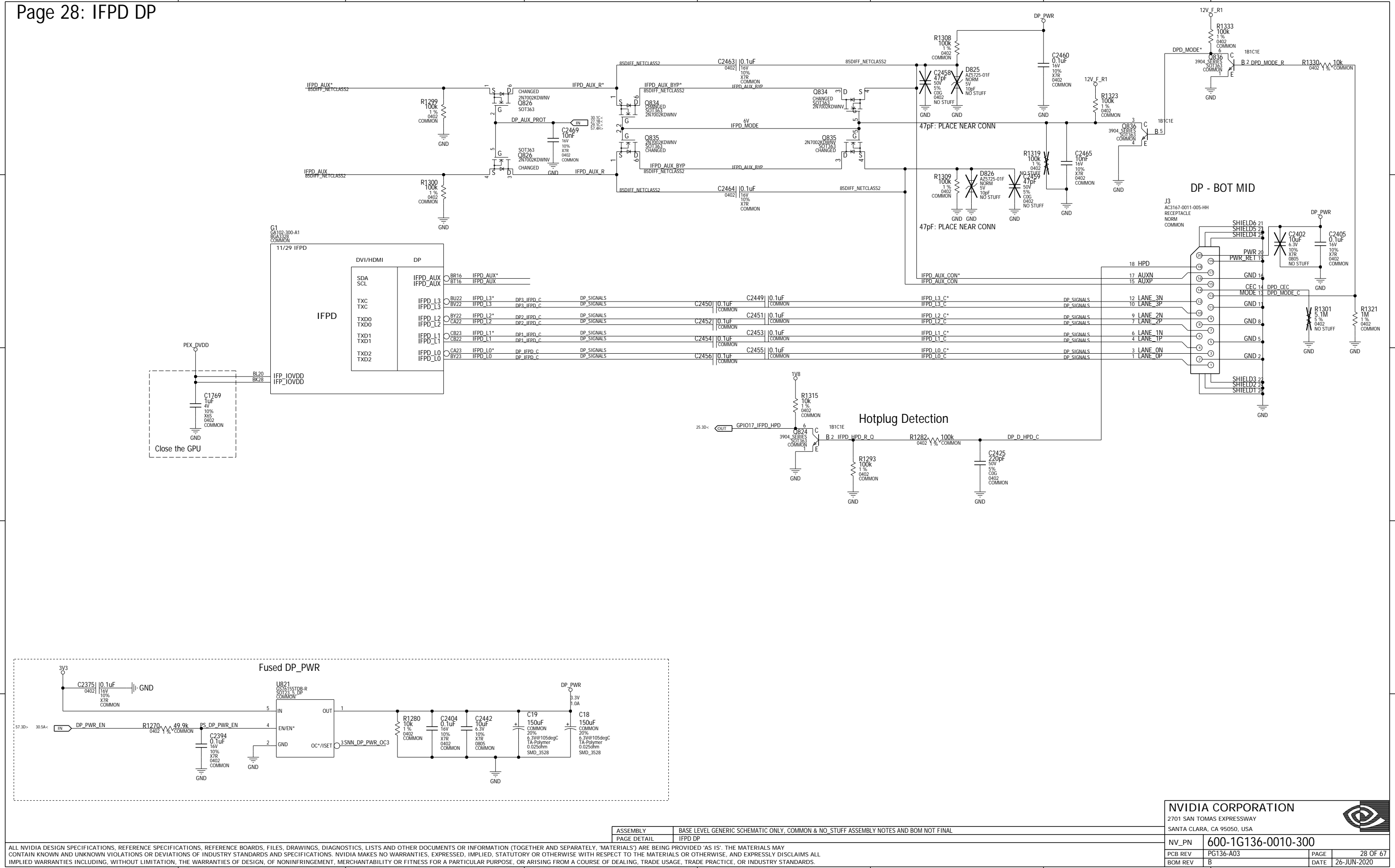
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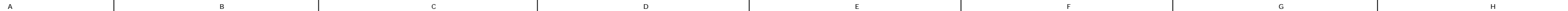
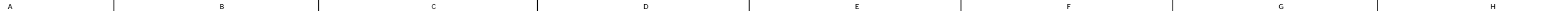
3

4

5







A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---

Page 31: MISC: ROM, Straps

GROUP0

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	H	00001
L	H	L	00010
L	H	H	00011
L	H	M	01101
H	H	H	00111

GROUP1

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	M	L	1001	FAN0/1=33%33%, FS_OVERT ENABLE

GROUP2

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

DEFAULT

<-DEFAULT

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default
SKU 200

STRAP0	CA7	STRAP0
STRAP1	CB7	STRAP1
STRAP2	BW8	STRAP2
STRAP3	BW7	STRAP3
STRAP4	BY7	STRAP4
STRAP5	BV8	STRAP5

ROM_CS
ROM_SI
ROM_SO
ROM_SCLK

OVERT

G1
CA102-300-A1
86A3328
COMMON

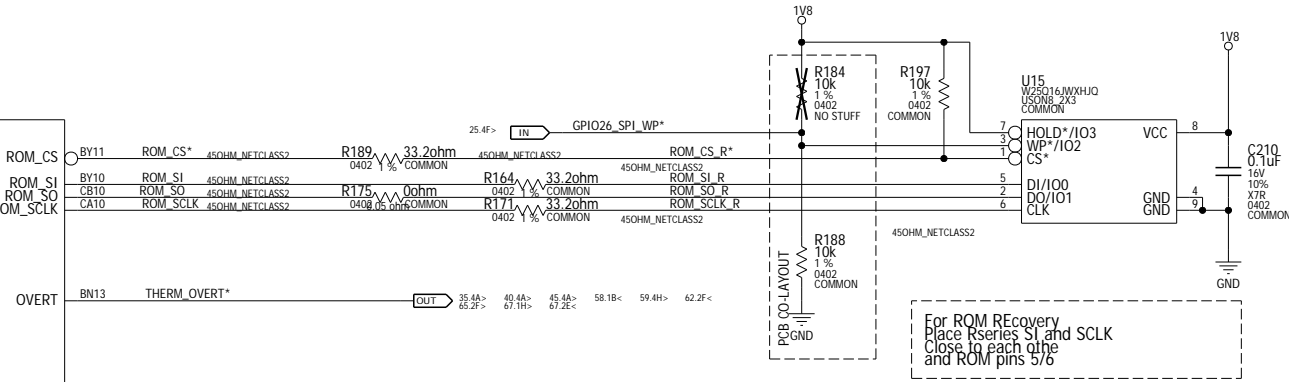
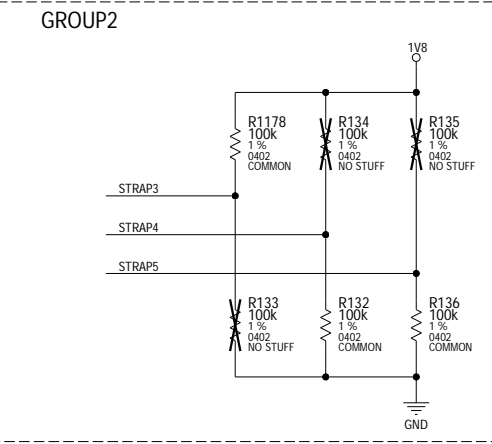
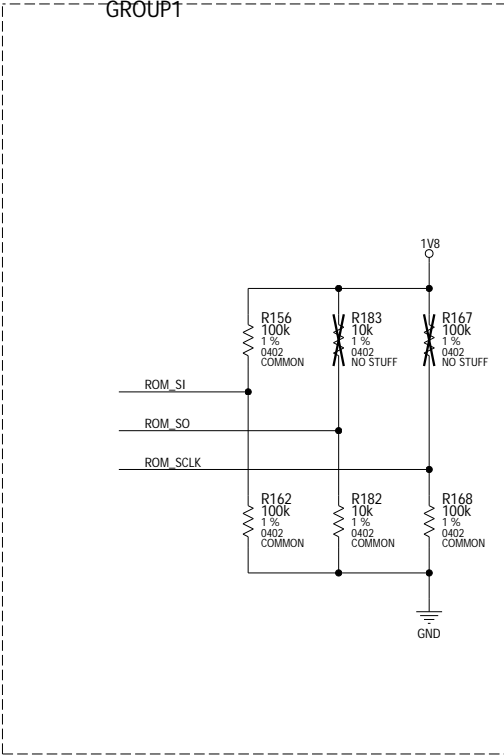
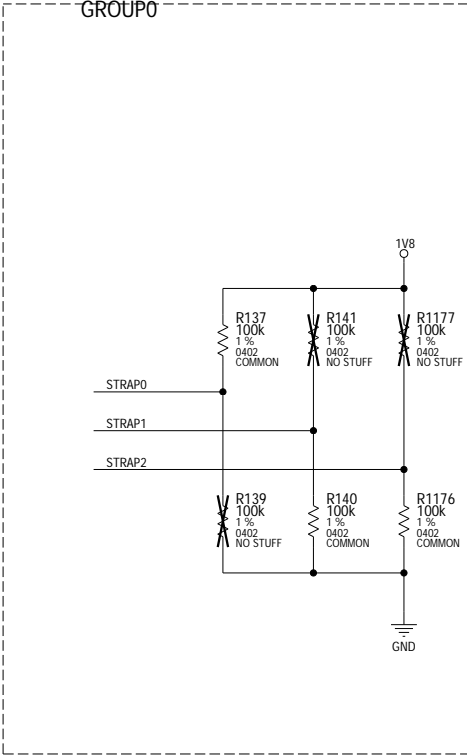
17/29 MISC2

ROM_CS
ROM_SI
ROM_SO
ROM_SCLK

OVERT

G1
CA102-300-A1
86A3328
COMMON

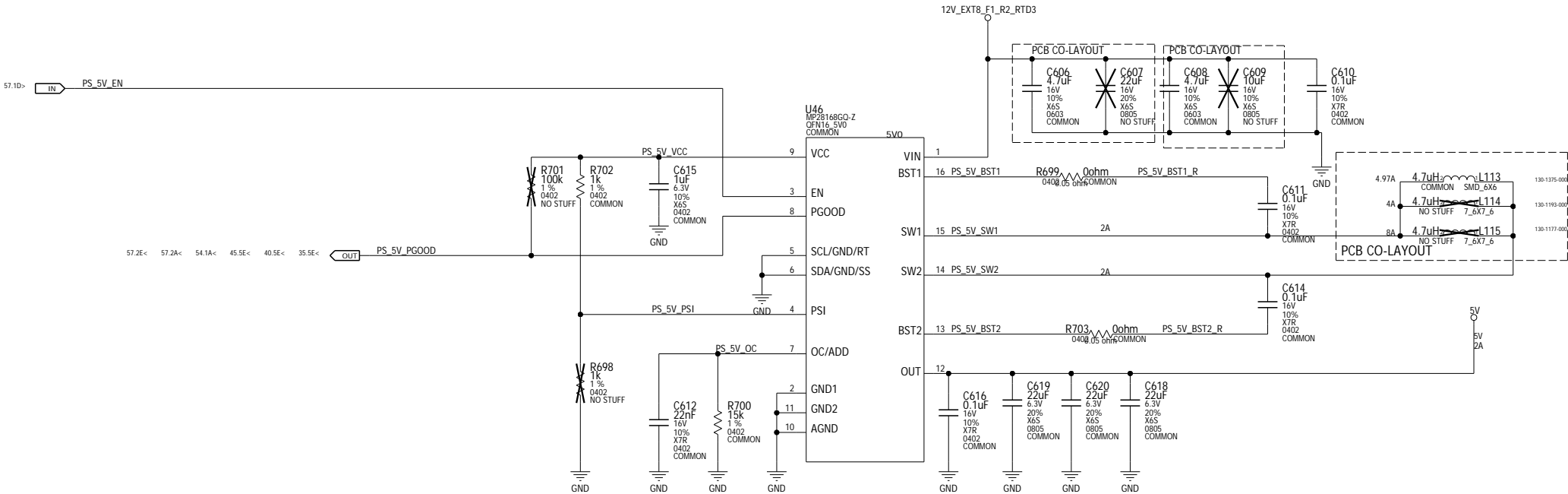
17/29 MISC2

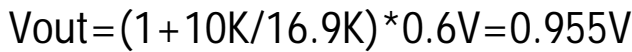


For ROM Recovery
Place Rseries SI and SCLK
Close to each other
and ROM pins 5/6

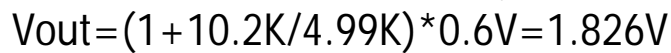
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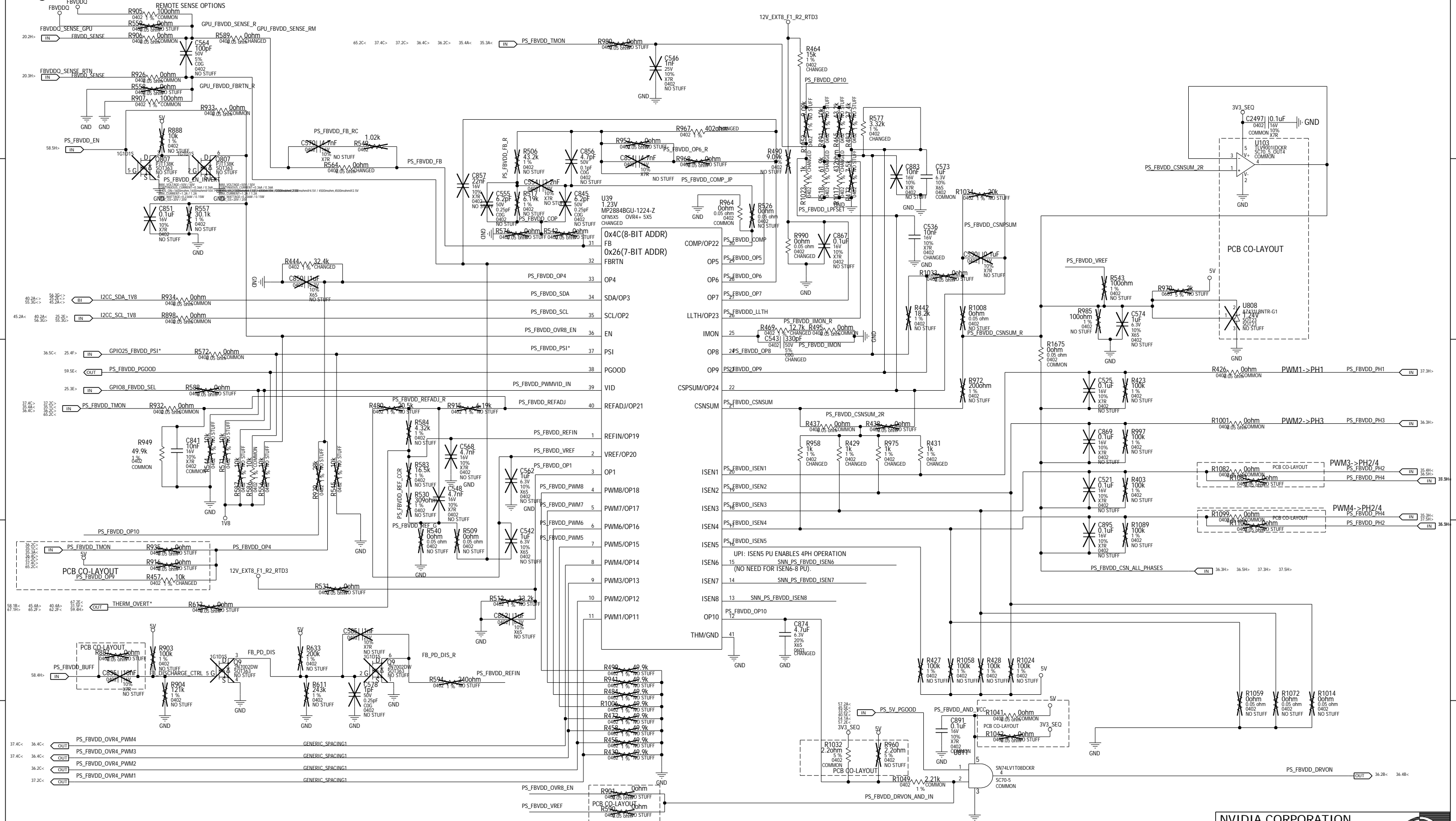
1V8

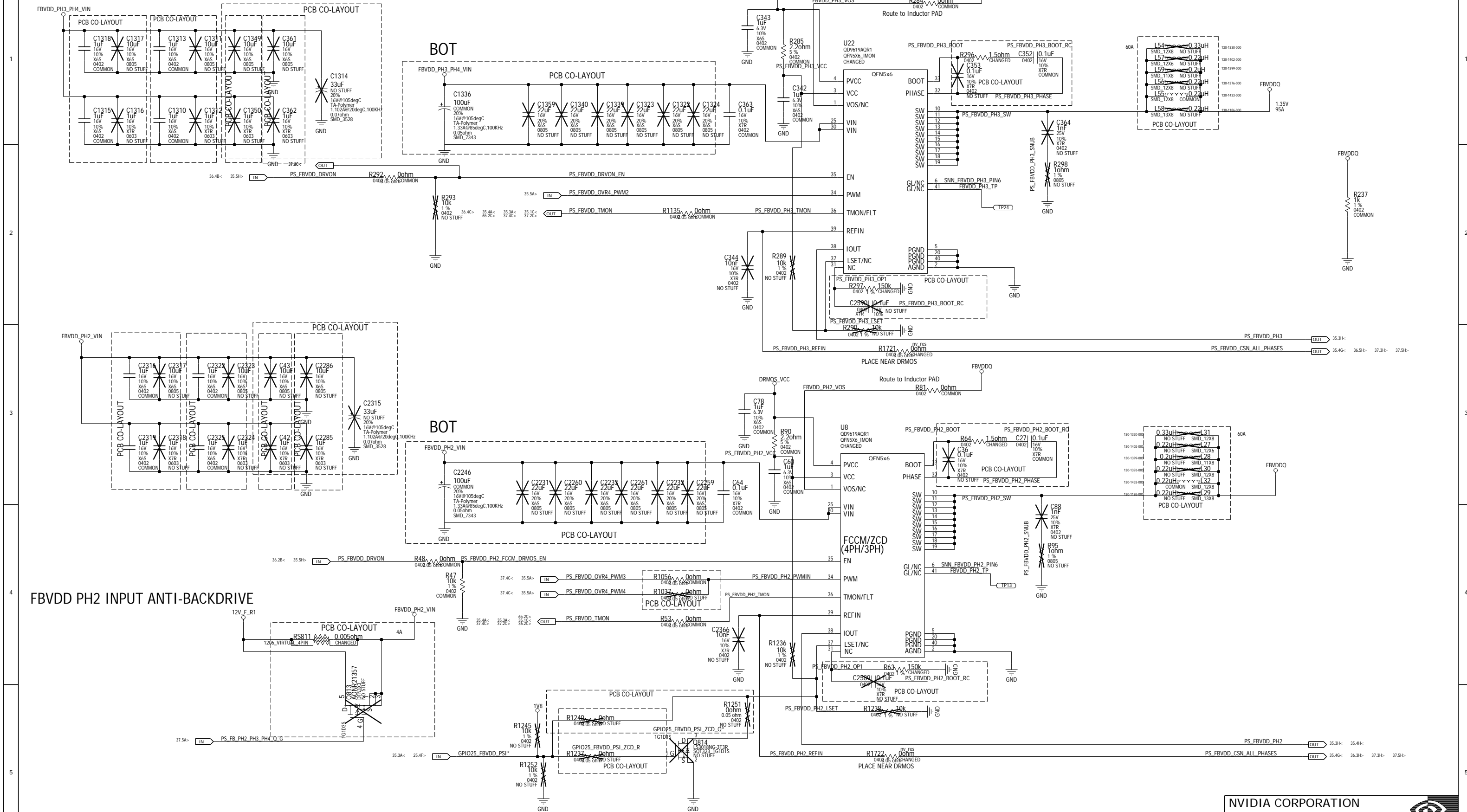


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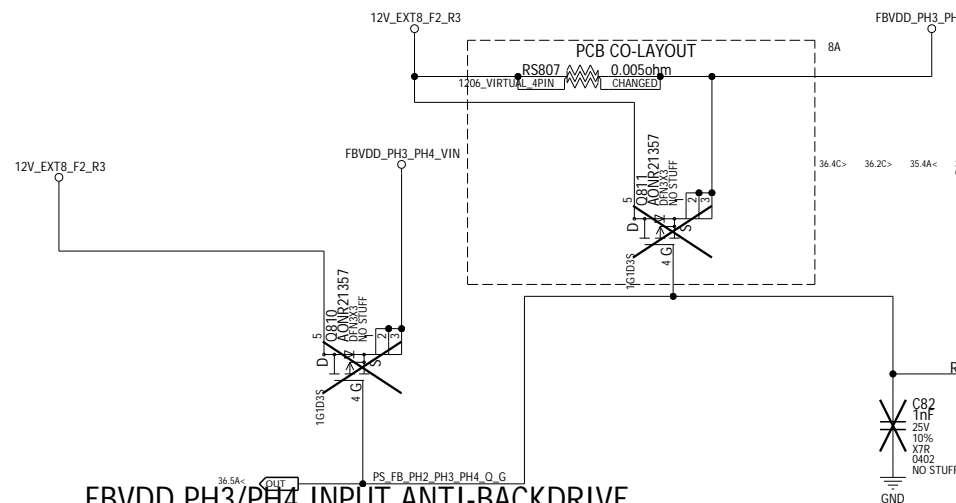
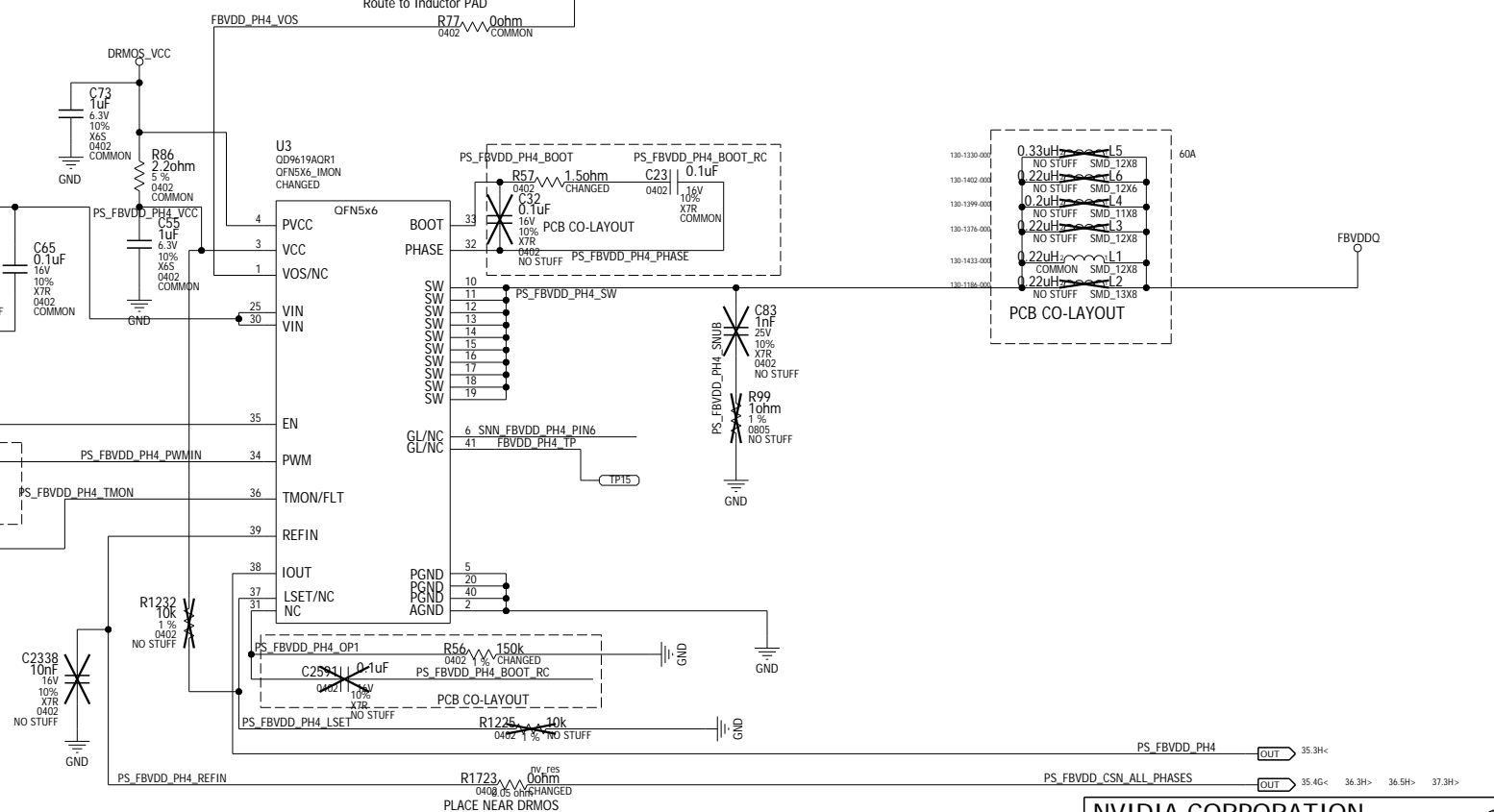
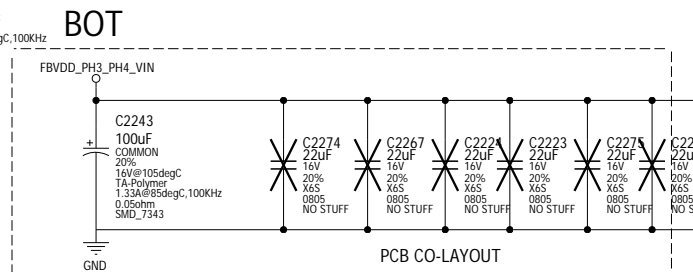
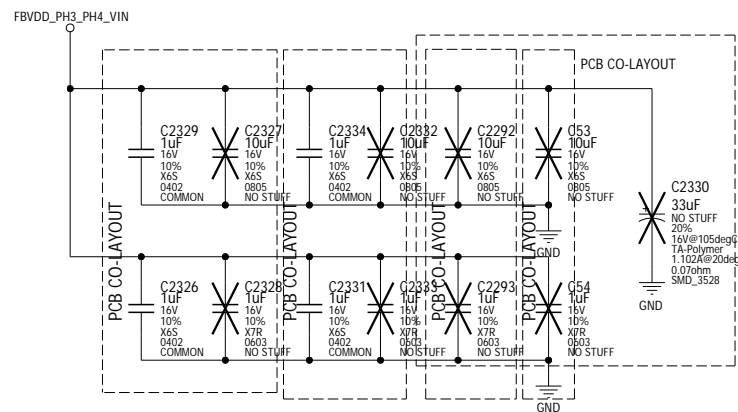
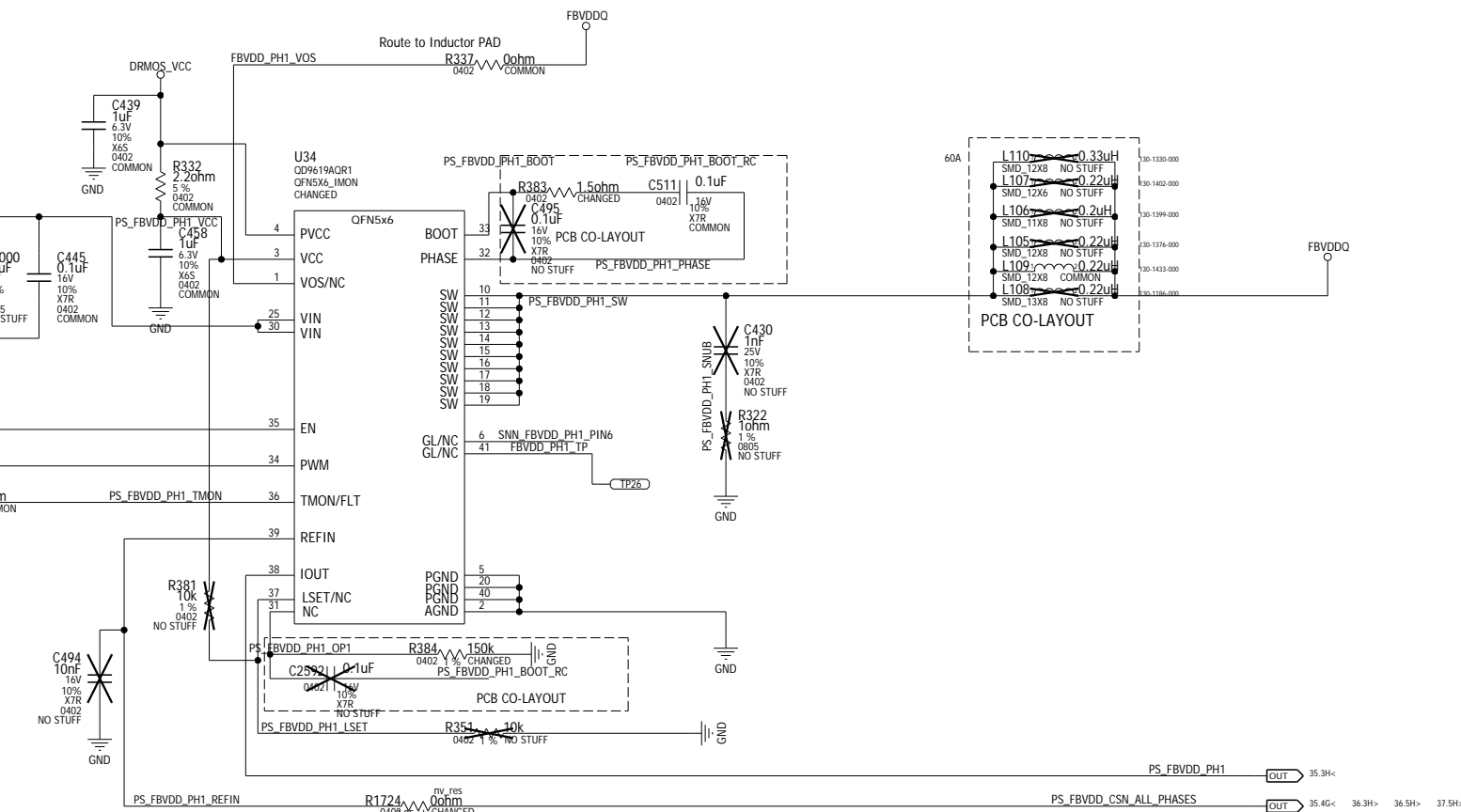
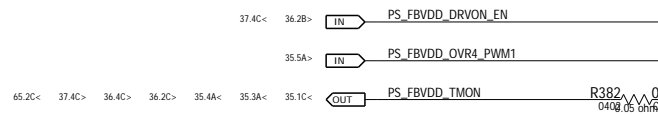
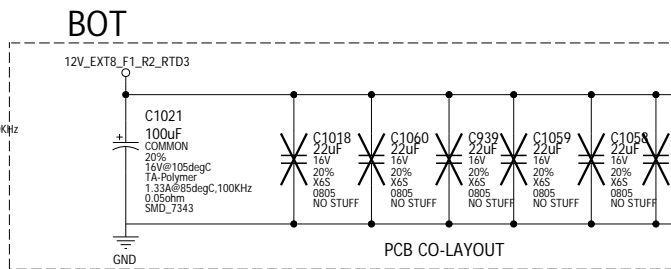
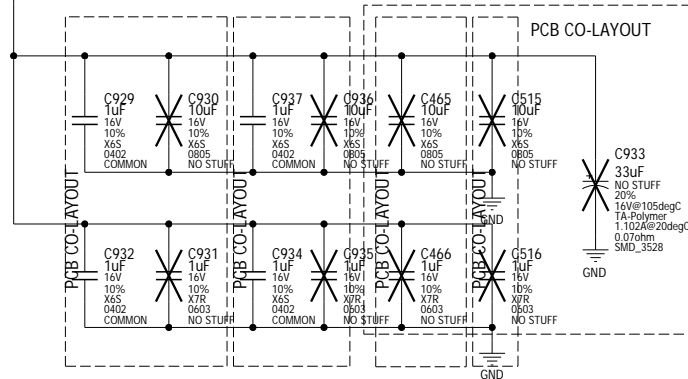
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Page 35: PS: FBVDD Controller






12V_EXT8_F1_R2_RTD3

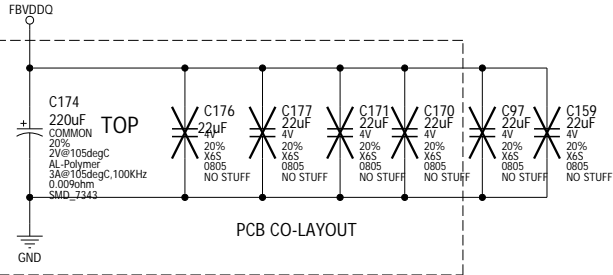


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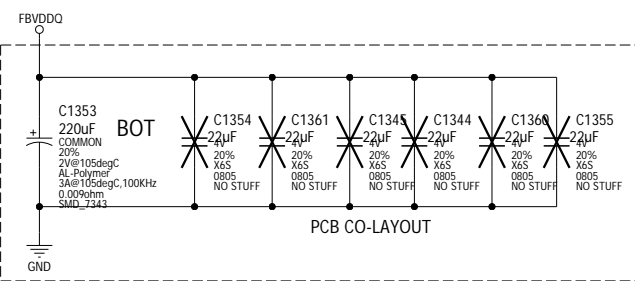
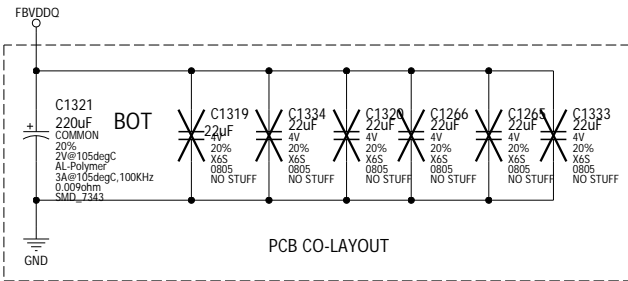
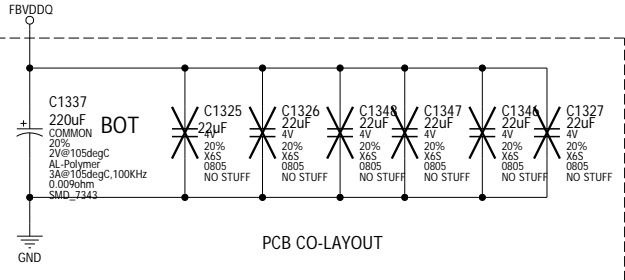
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: FBVDD PH1 (PWM1) and PH4 (PWM3/4)

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN PCB REV BOM REV		600-1G136-0010-300 P136-A03 B		
		PAGE DATE	37 OF 67 26-JUN-2020	

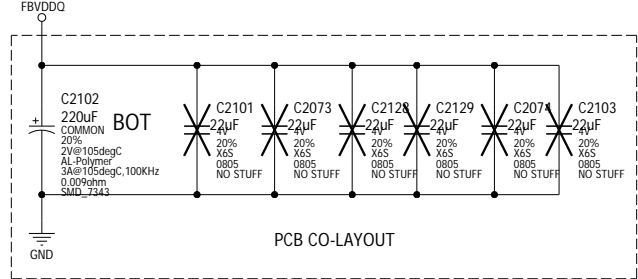
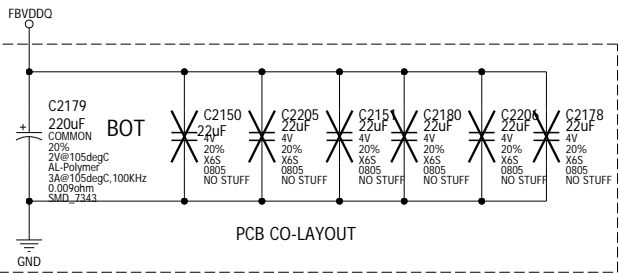
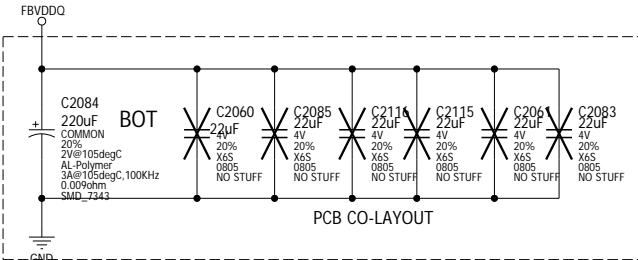
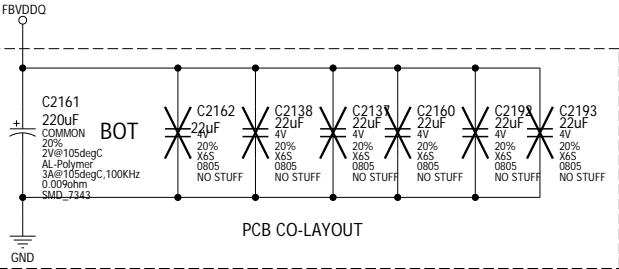
PLACE NEAR POWER SUPPLY
8x SMD7343 330uF CO-LAYOUT WITH 48x 0805 22uF



TOP WEST OF PCB

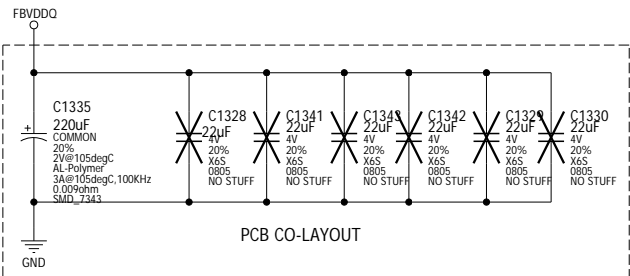
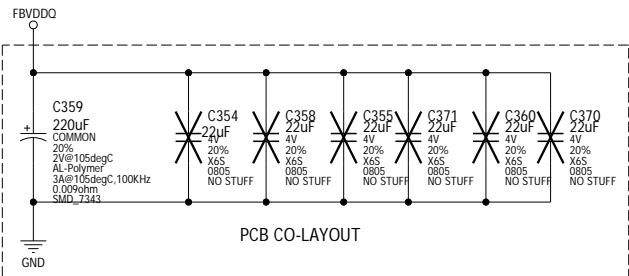
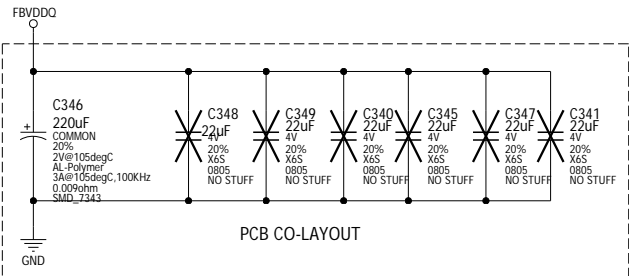
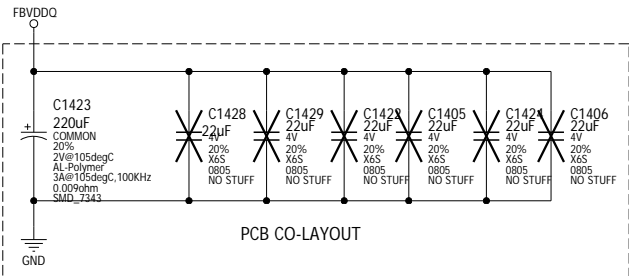
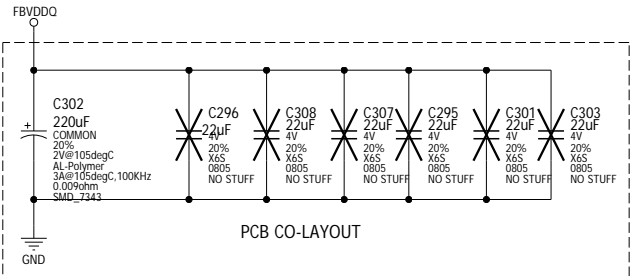
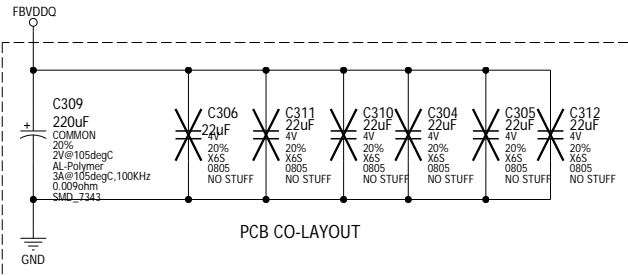
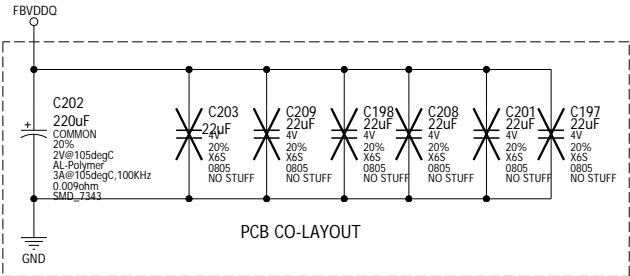
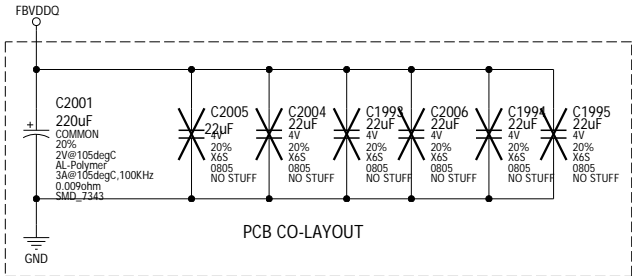


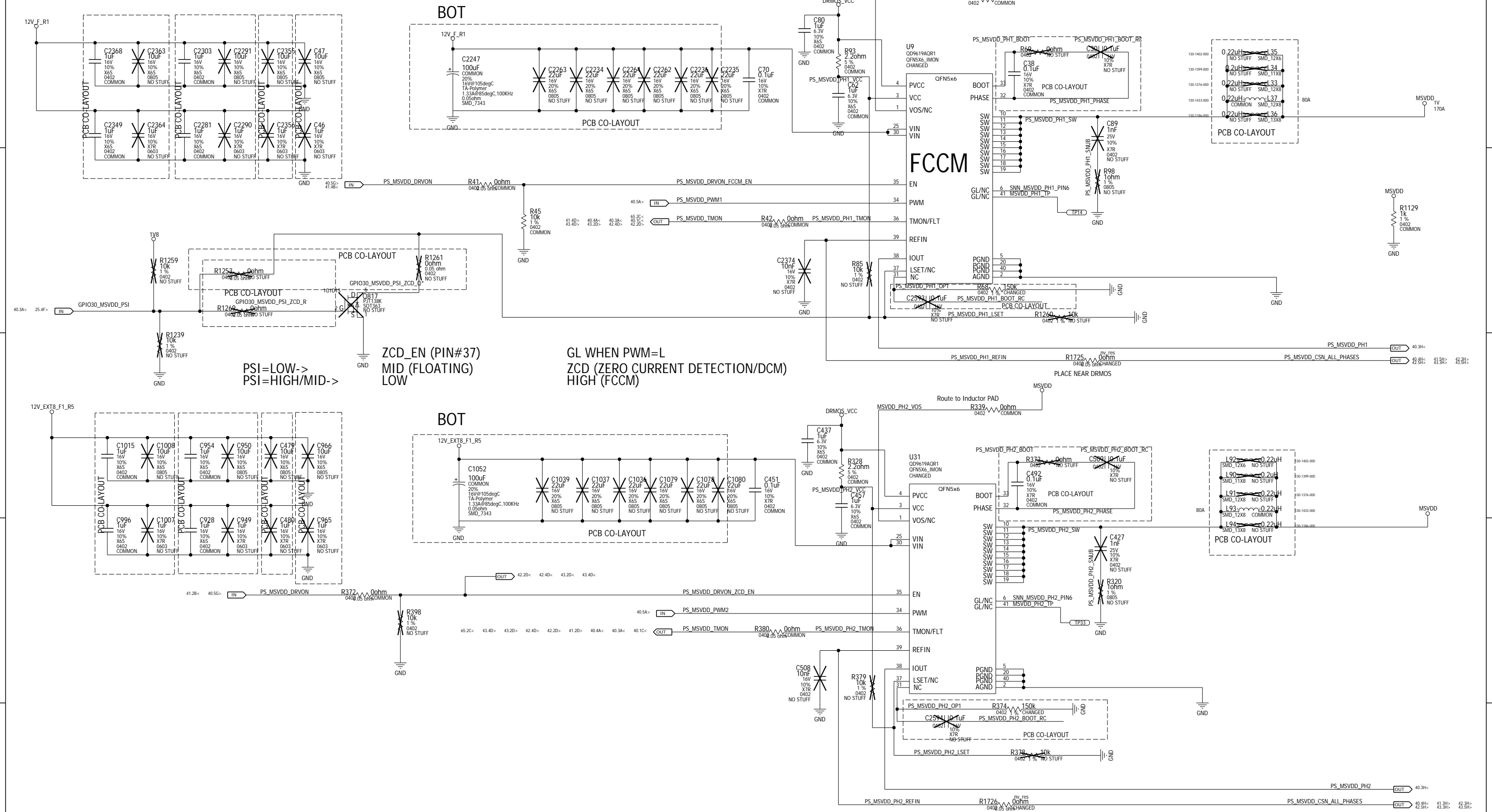
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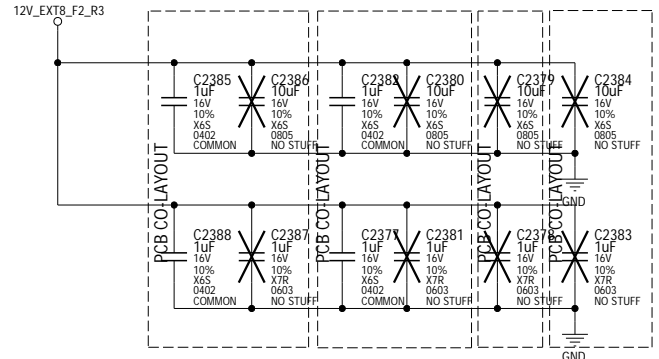
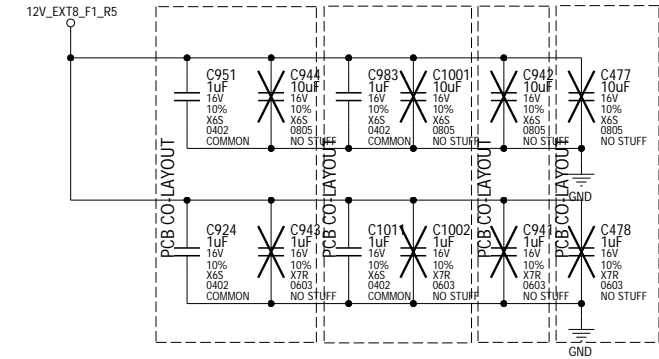
BACK EAST OF PCB

PLACE NEAR MEMORY

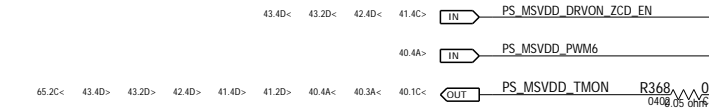
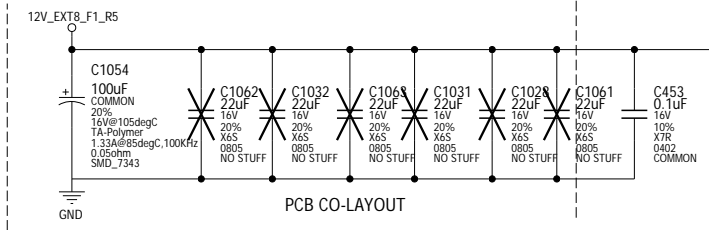




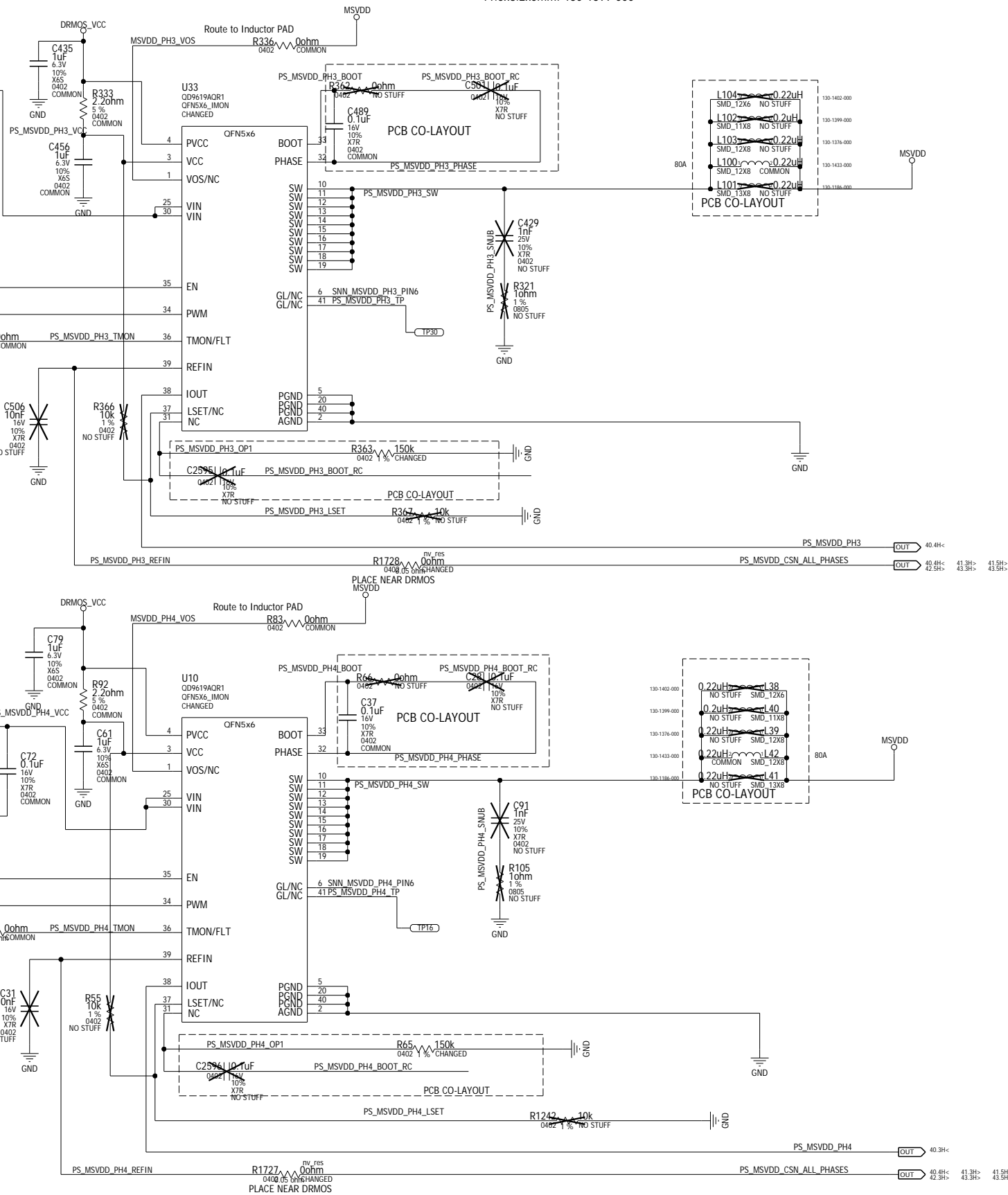
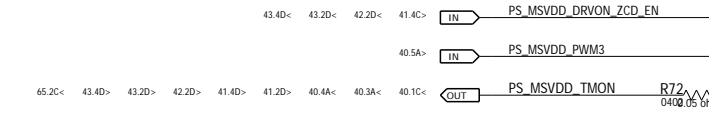
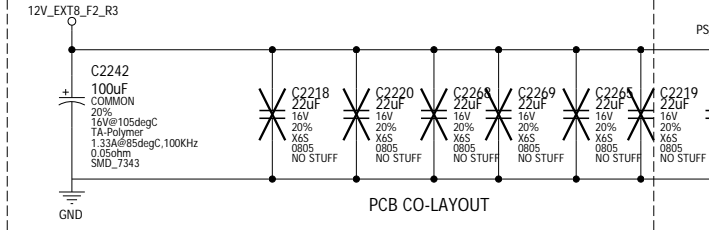
11.5x8.2x5mm: 130-1399-000



BOT



BOT



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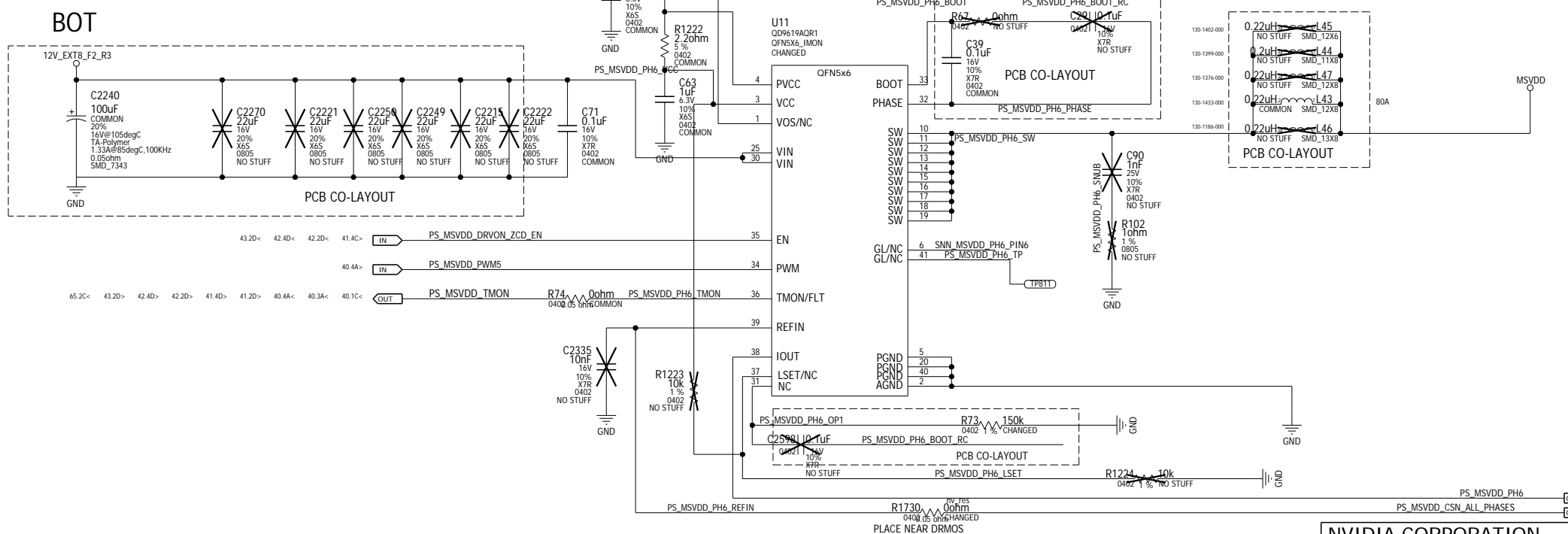
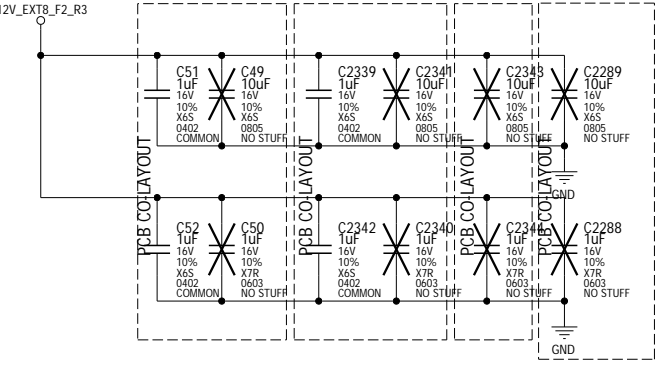
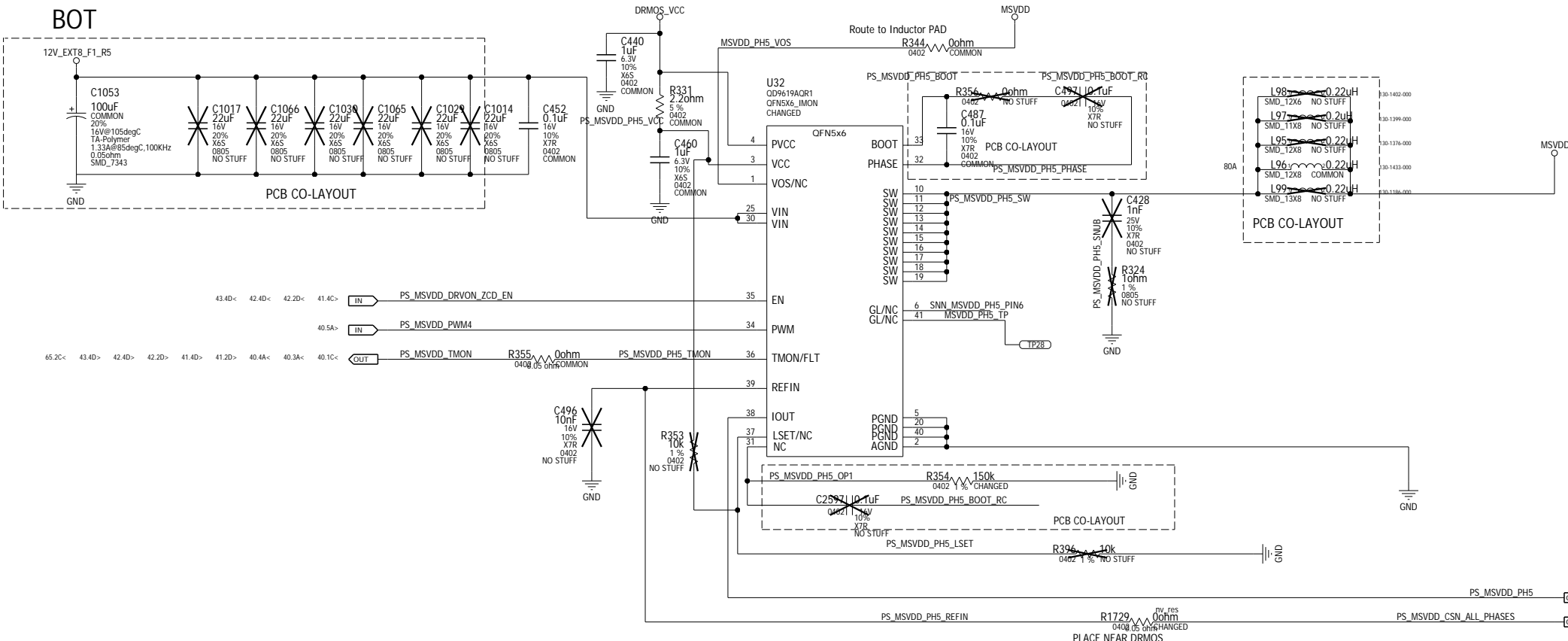
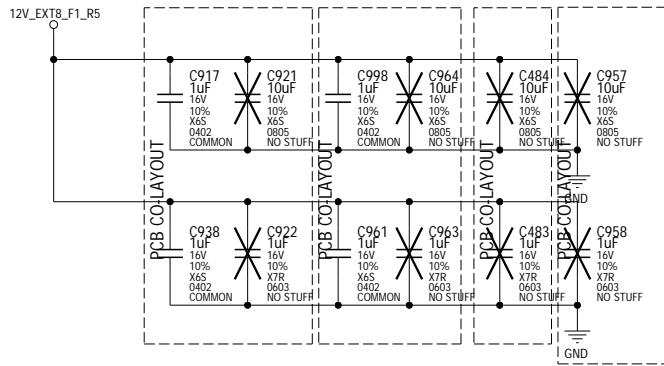
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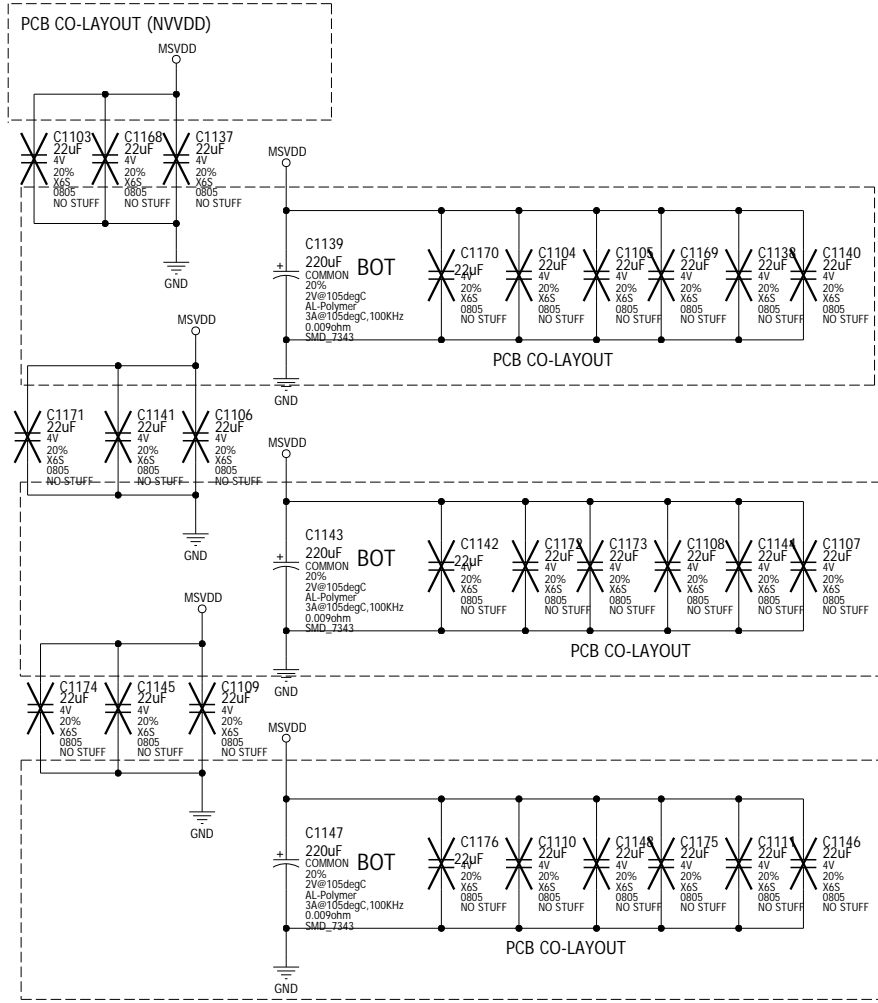
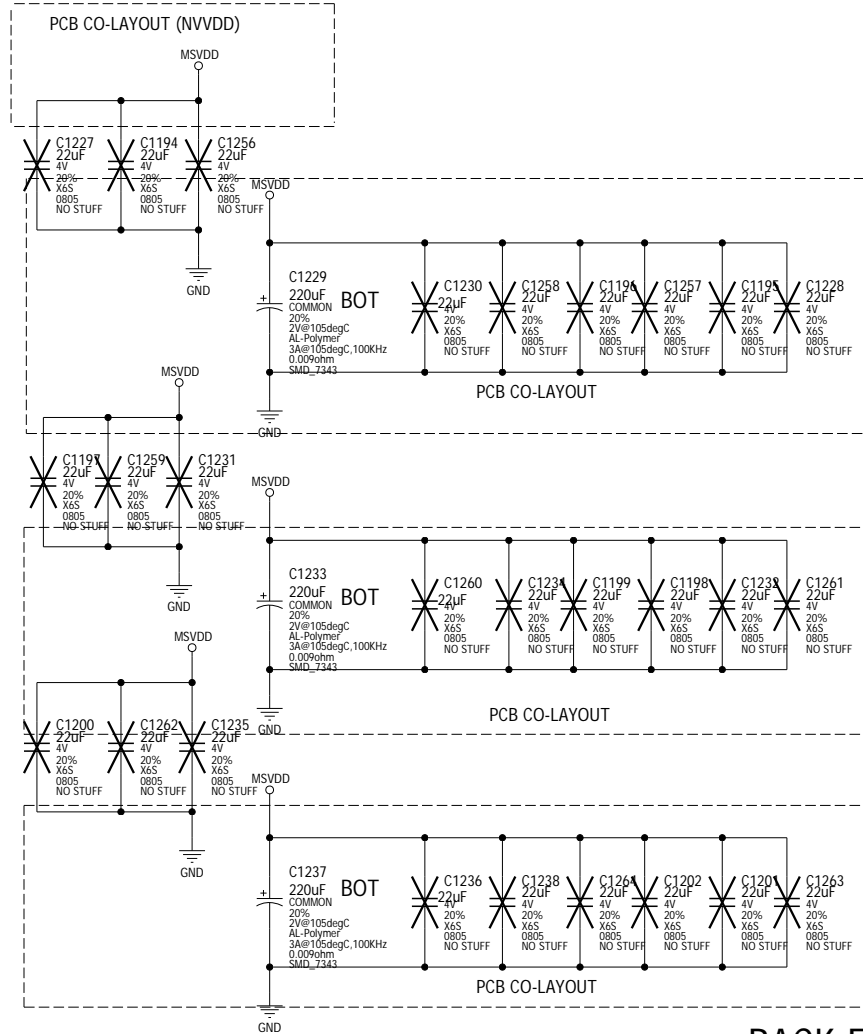
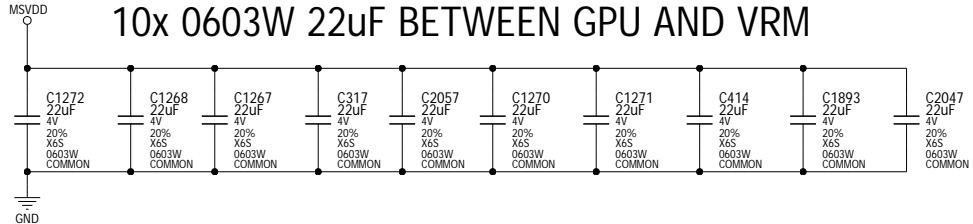
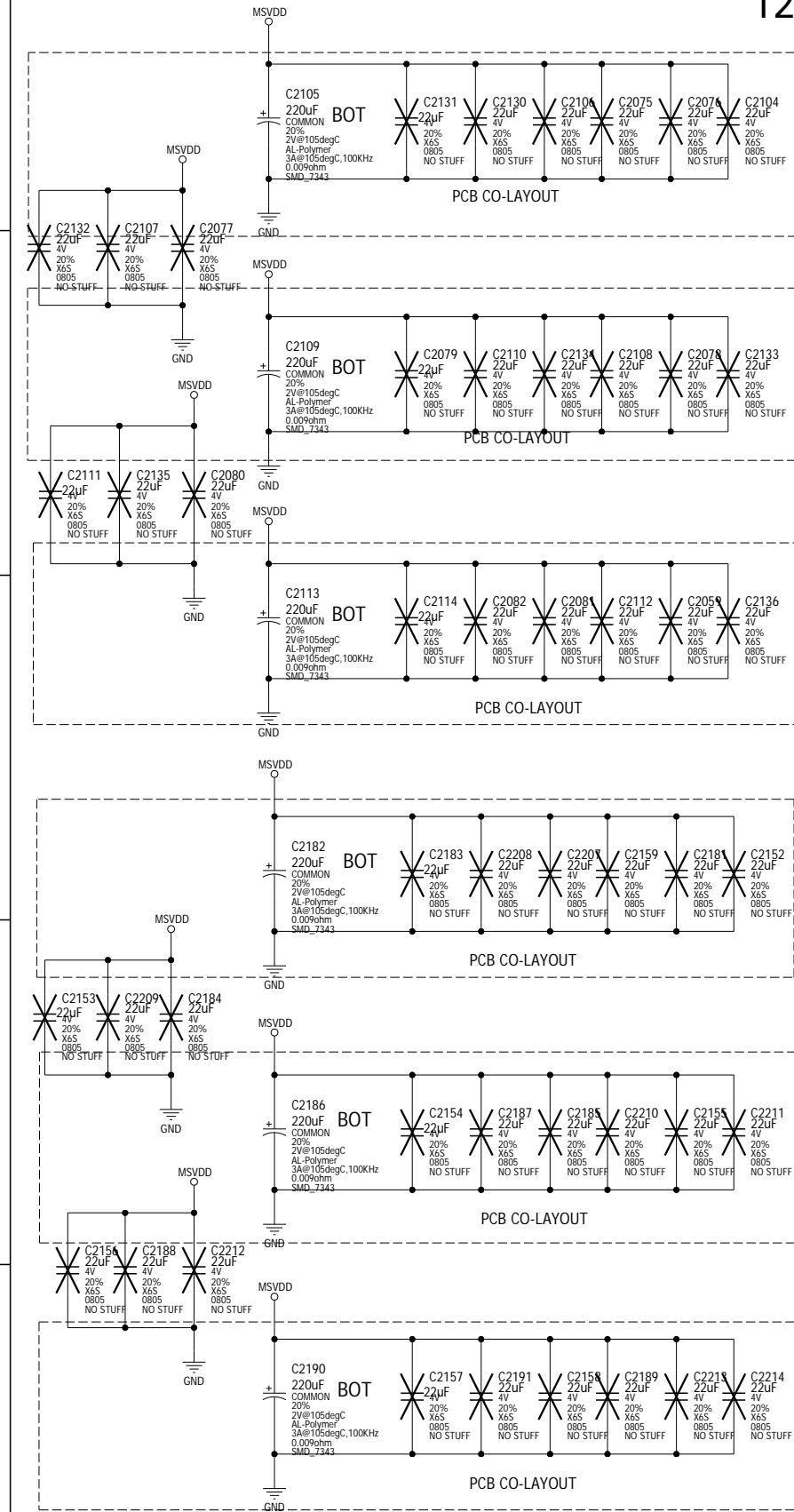
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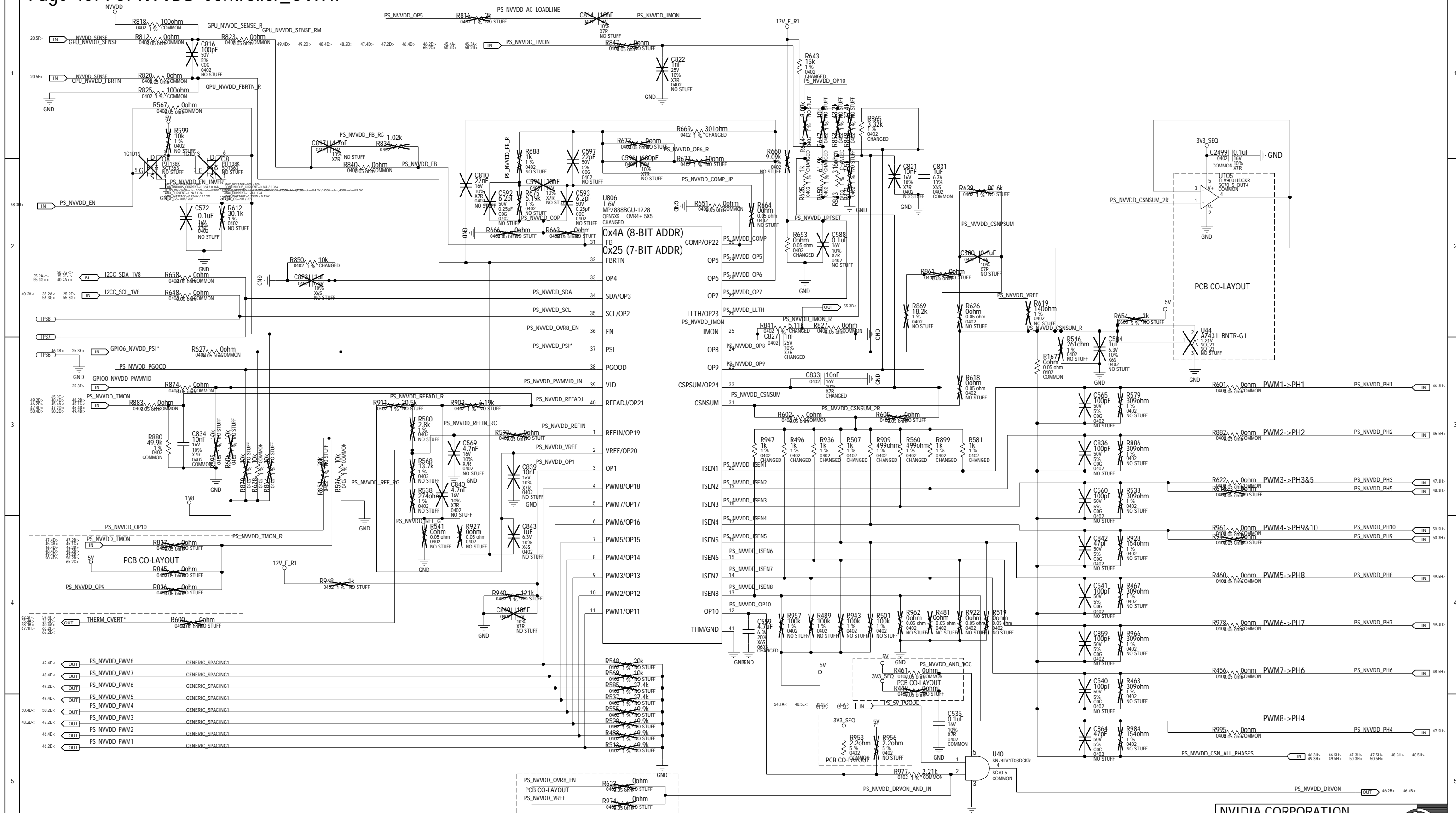


12x SMD7343 330uF CO-LAYOUT WITH 72x 0805 22uF



BACK EAST OF PCB

Page 45: PS: NVVDD Controller_OVR4i



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD CONTROLLER OVR4i

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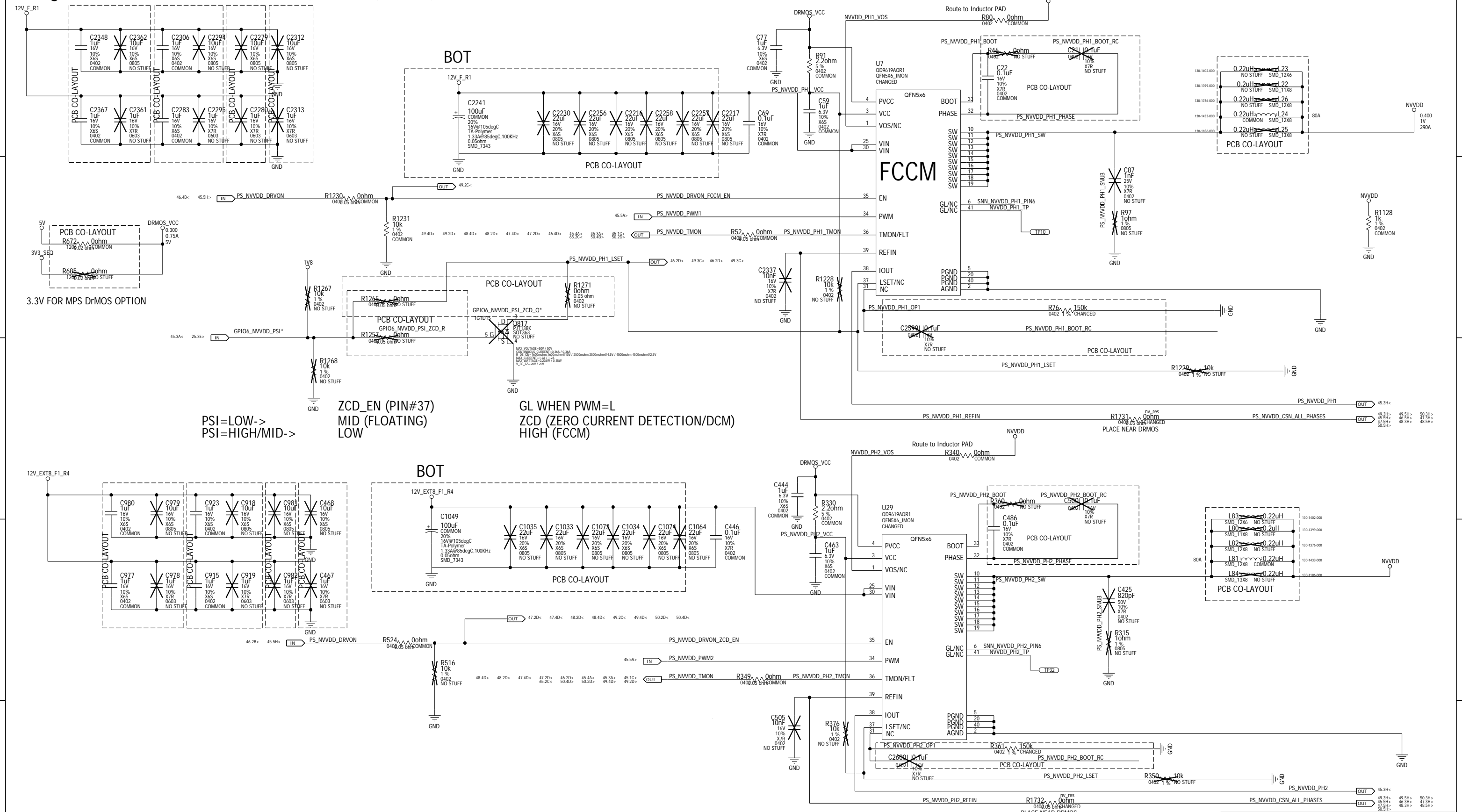
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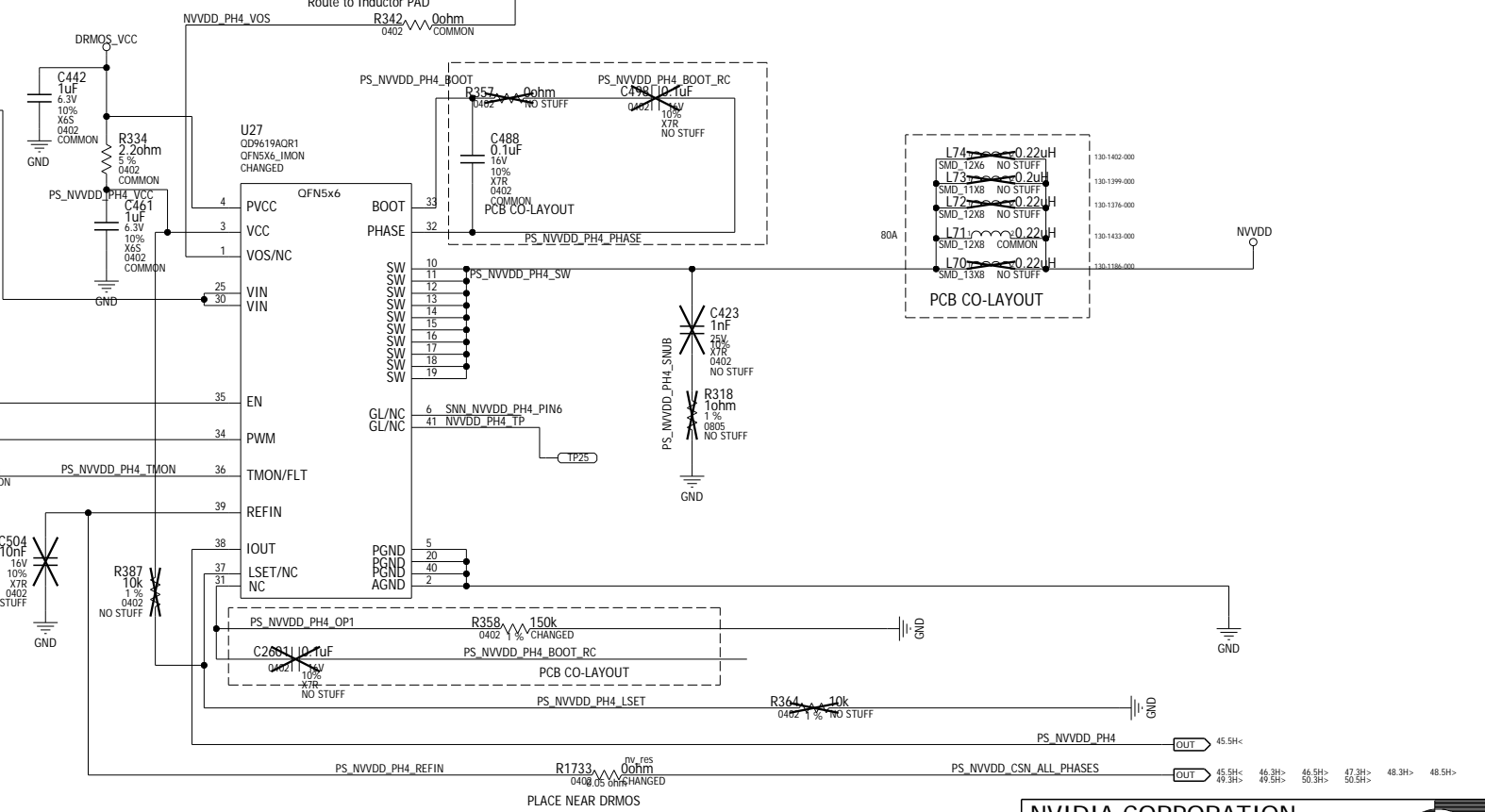
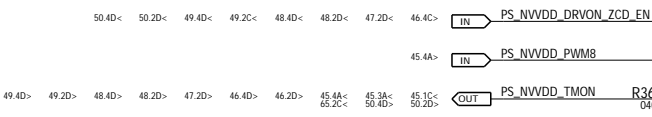
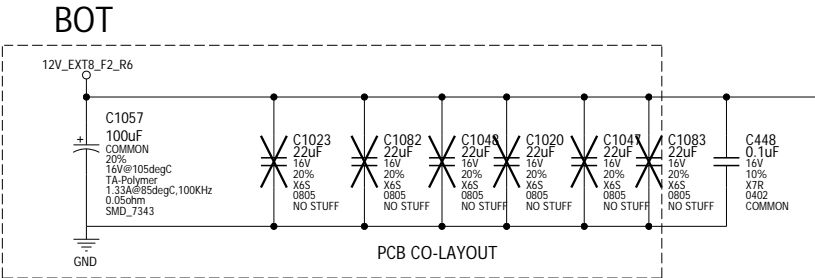
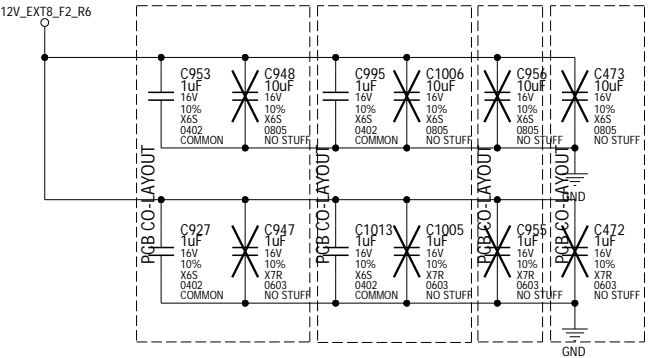
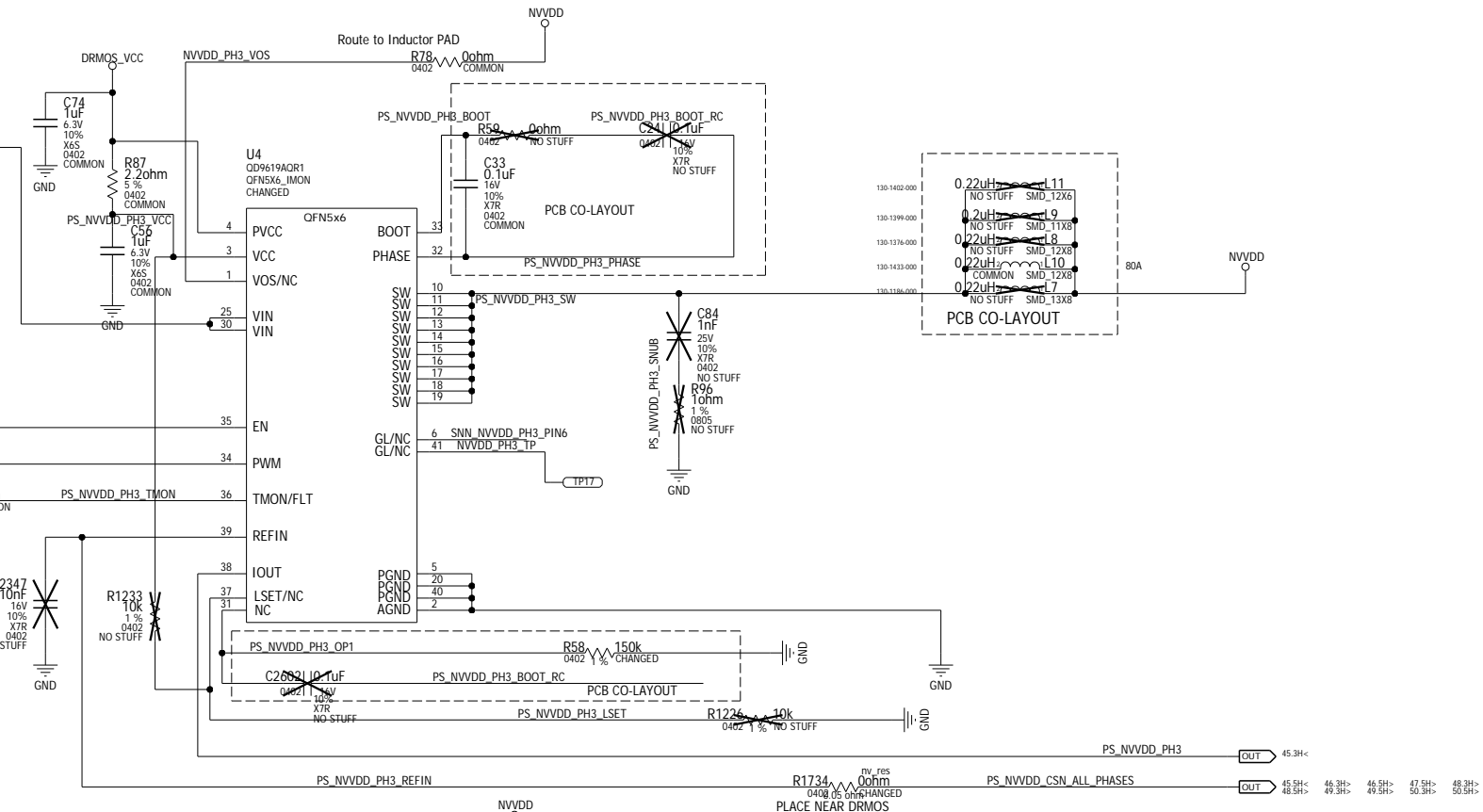
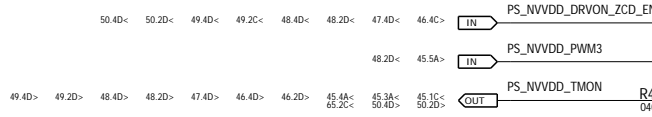
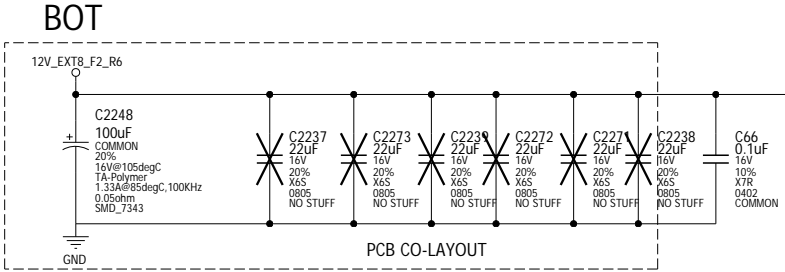
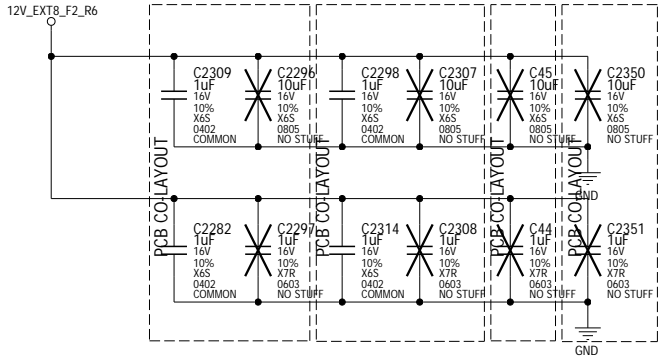


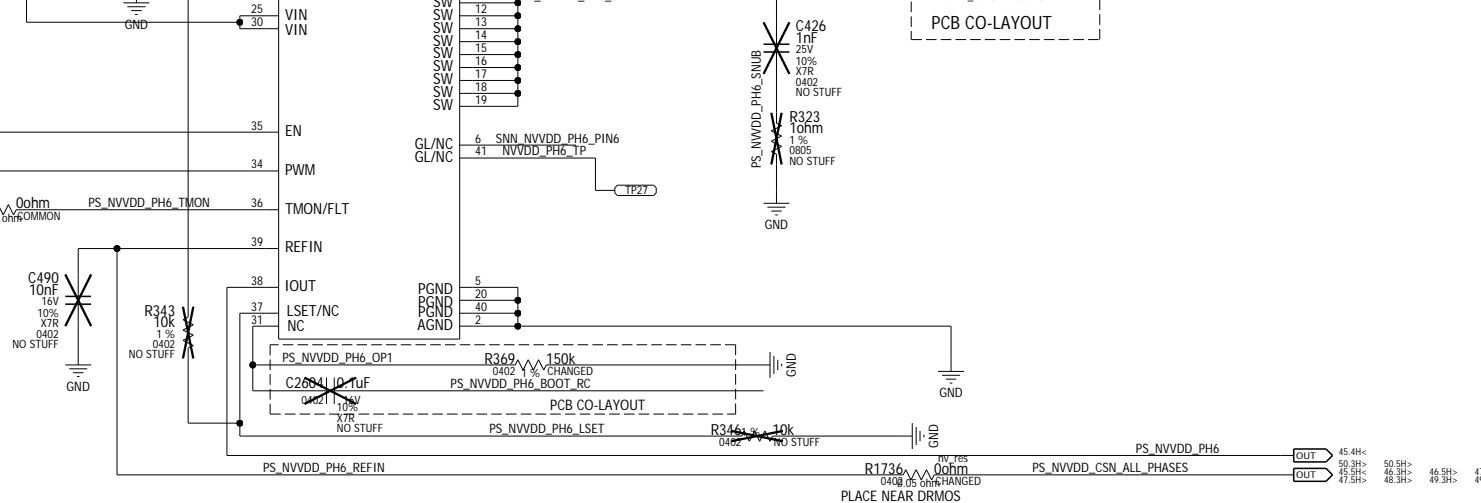
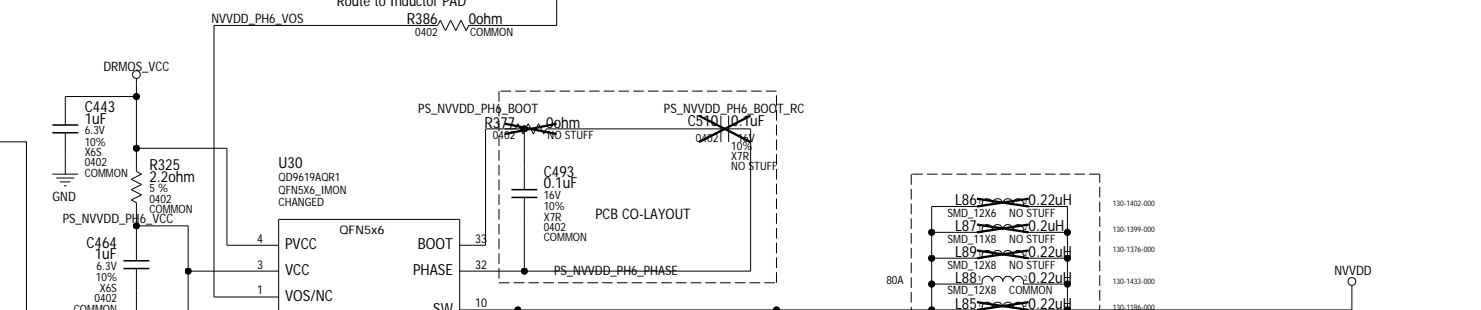
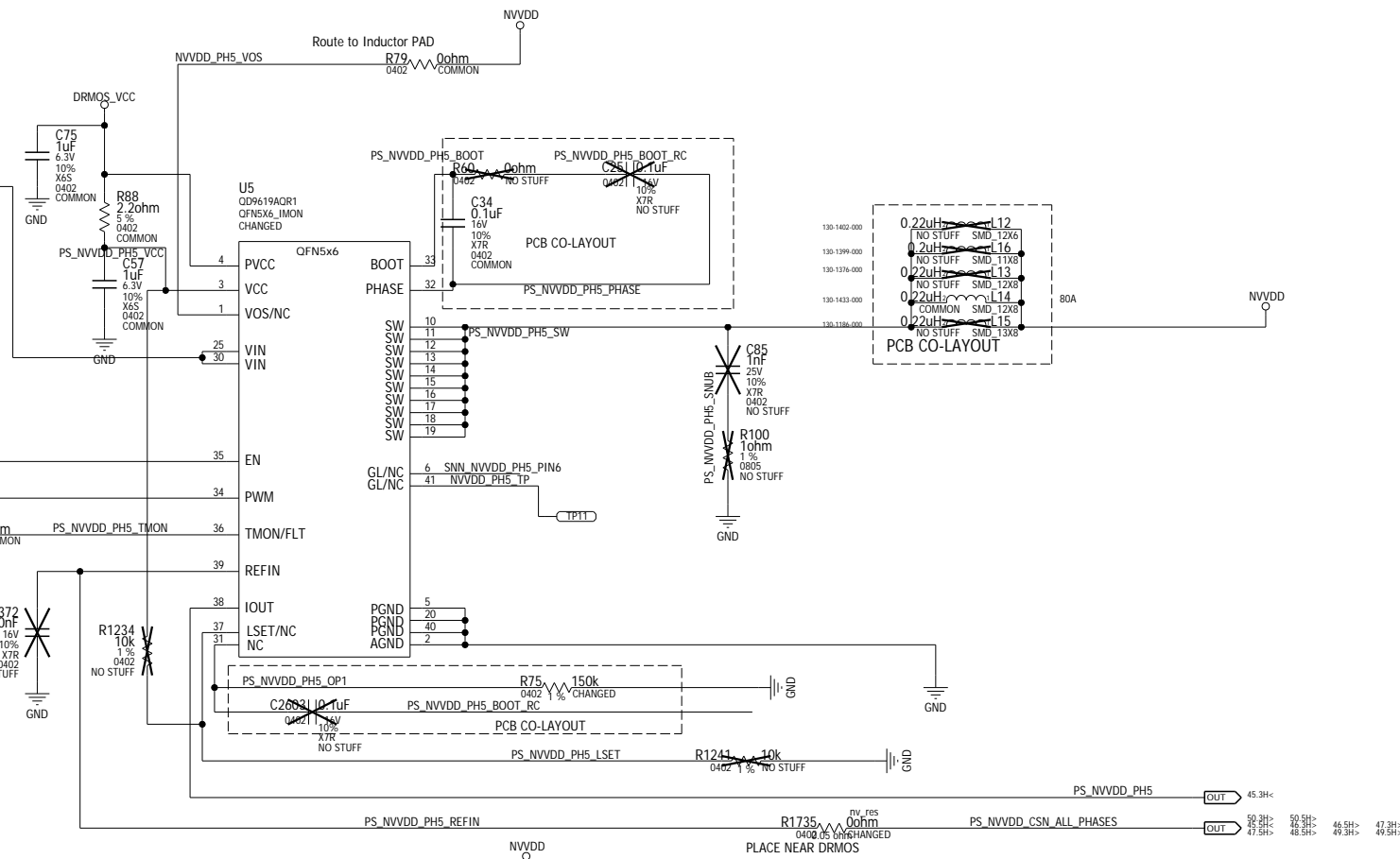
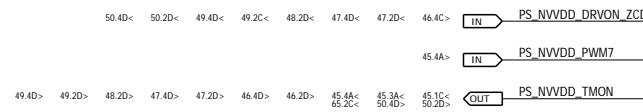
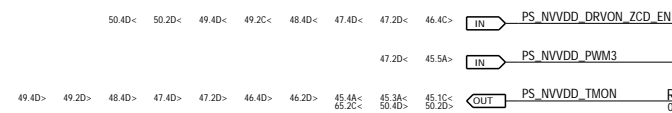
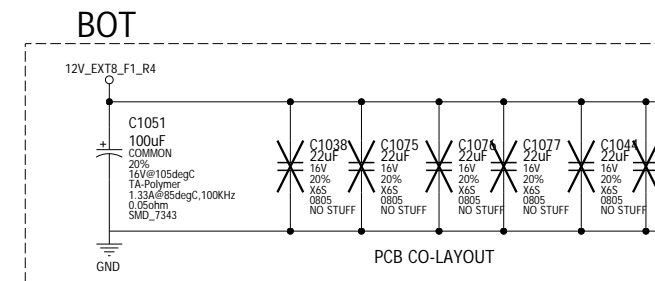
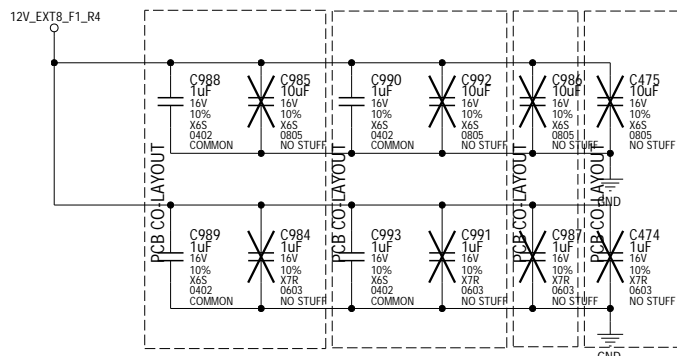
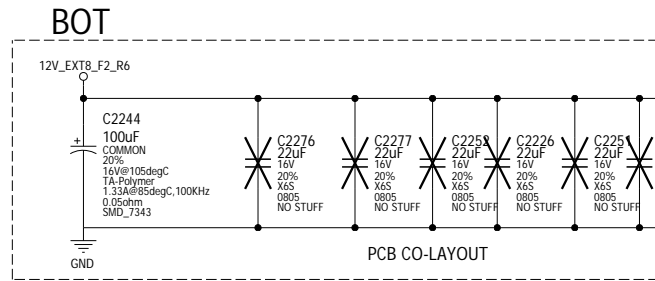
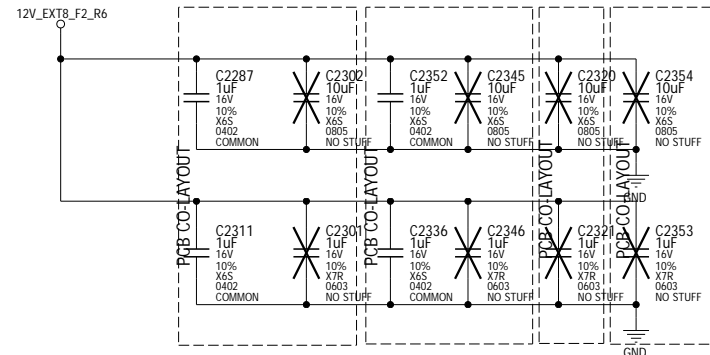
NV_PN	600-1G136-0010-300
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Page 46: PS: NVVDD PH 1 (PWM1), PH 2 (PWM2)







ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD PH5 (PWM3) and PH6 (PWM7)

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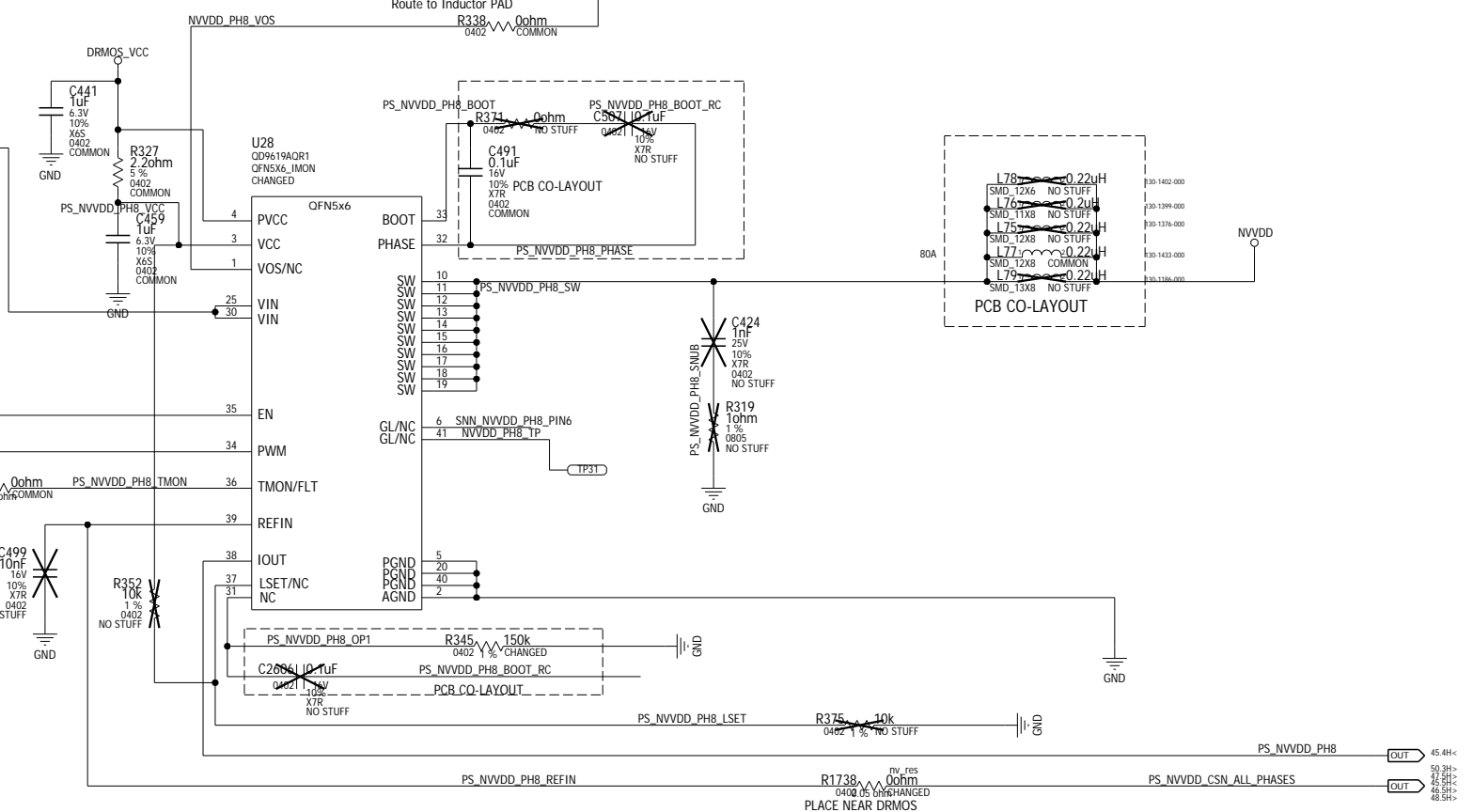
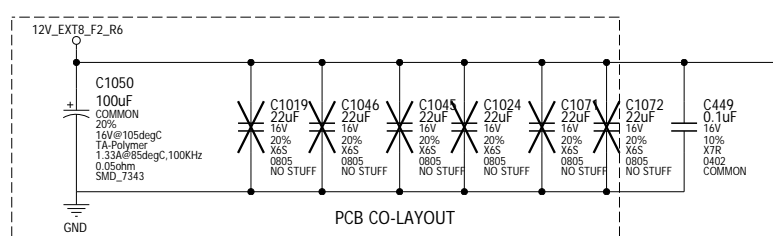
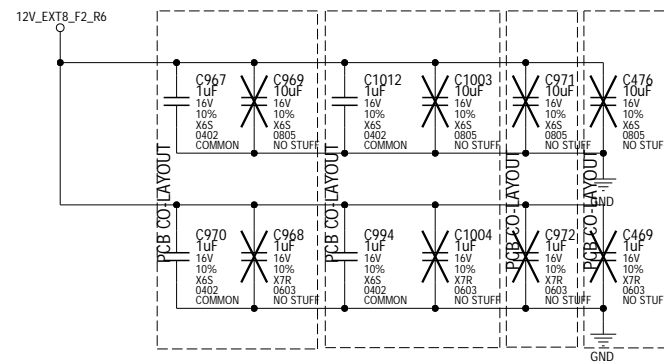
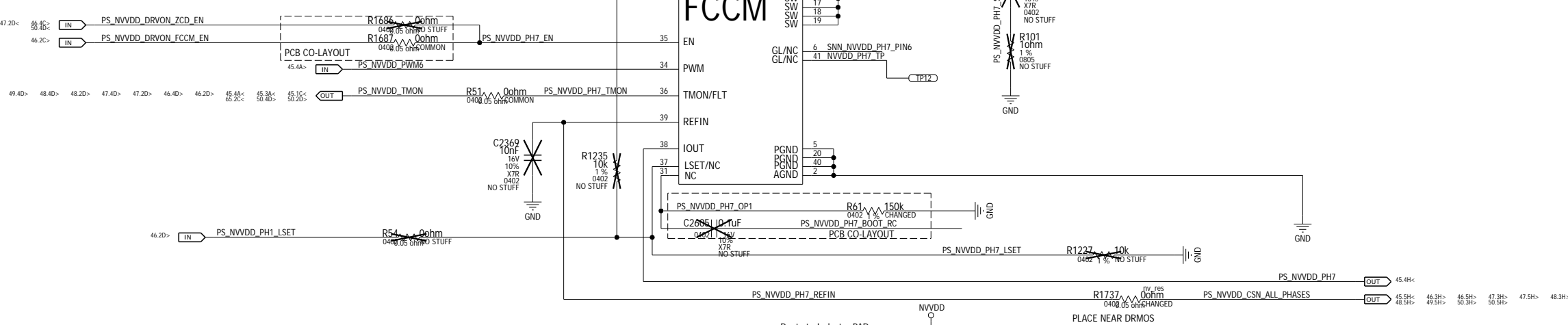
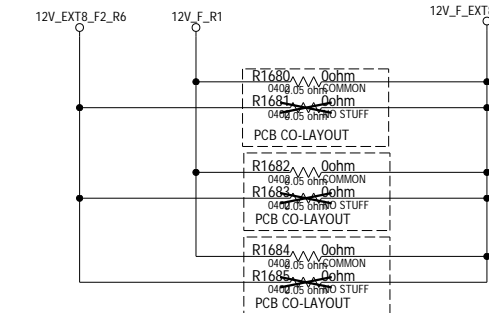
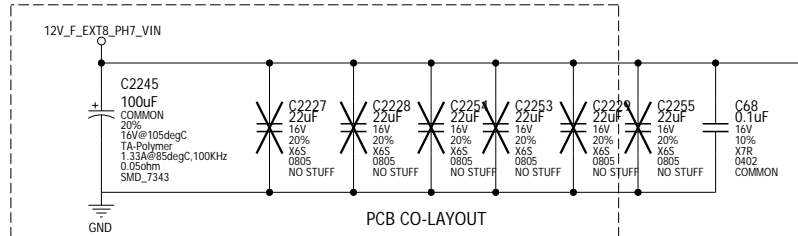
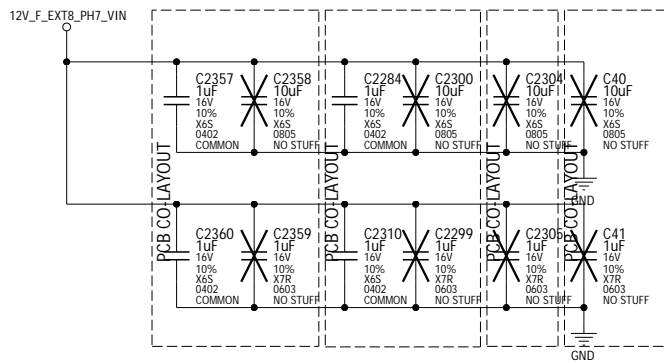


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Page 49: PS: NVVDD PH 7 (PWM6), PH8 (PWM5)



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD PH7 (PWM6) and PH8 (PWM5)

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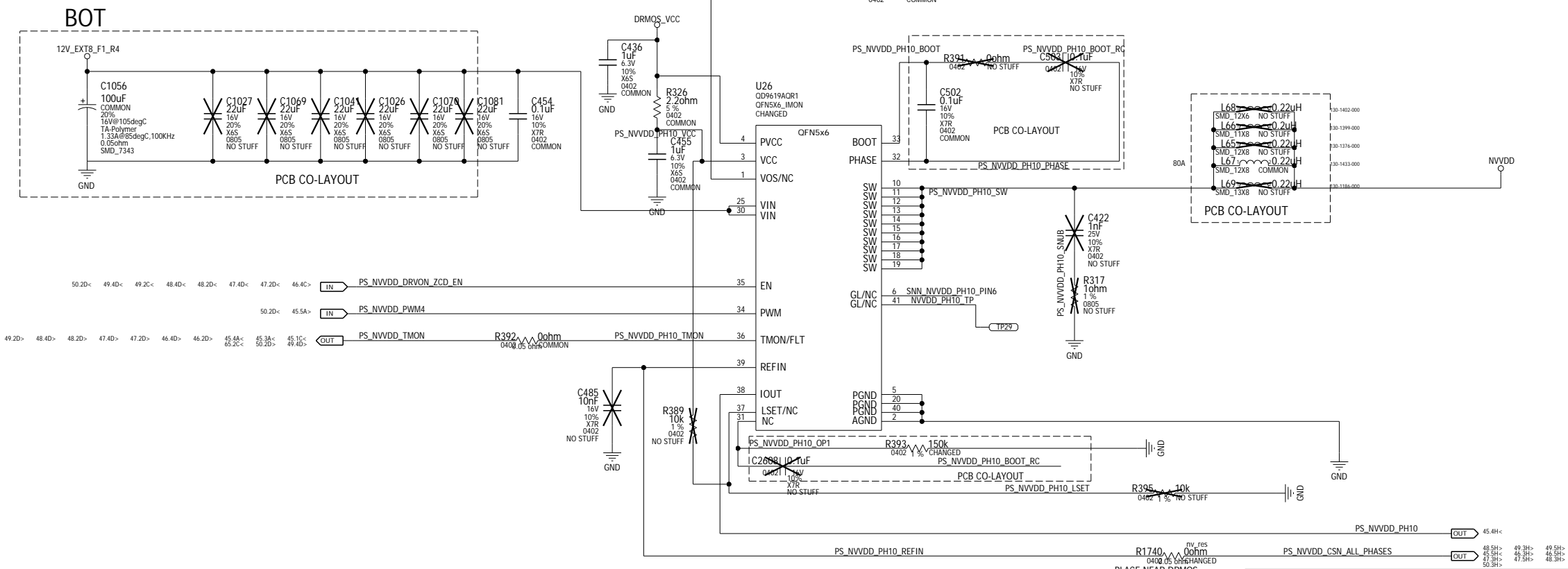
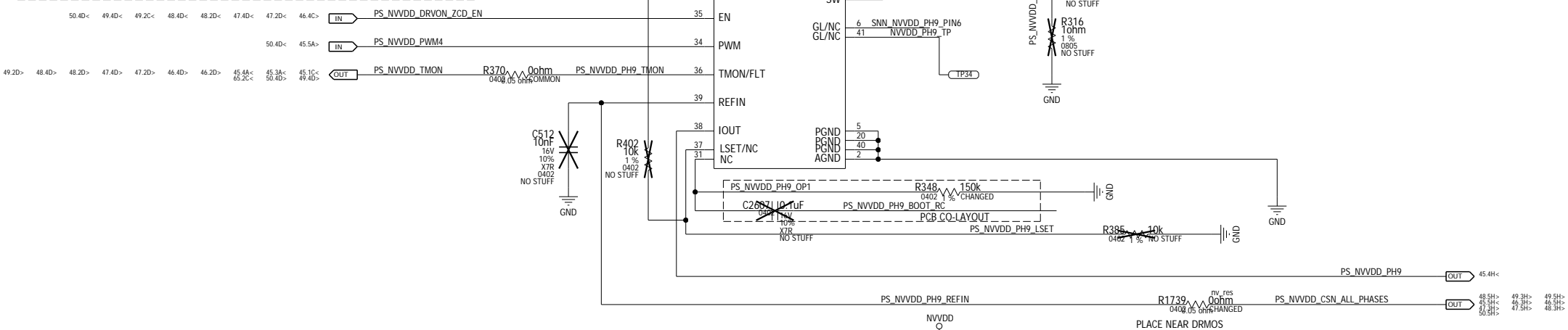
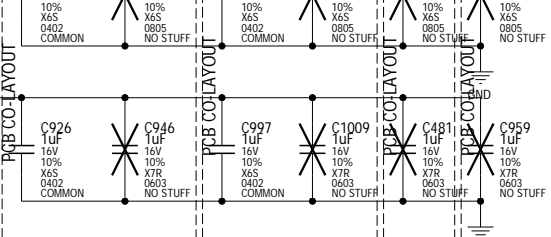
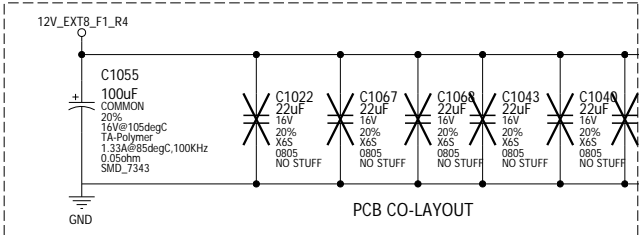
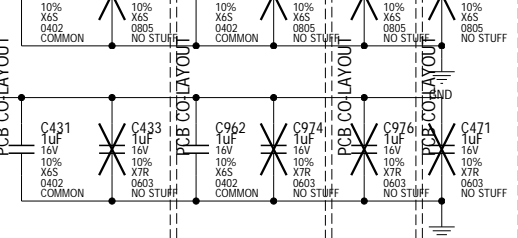
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD PH9 (PWM4), PH10 (PWM4)

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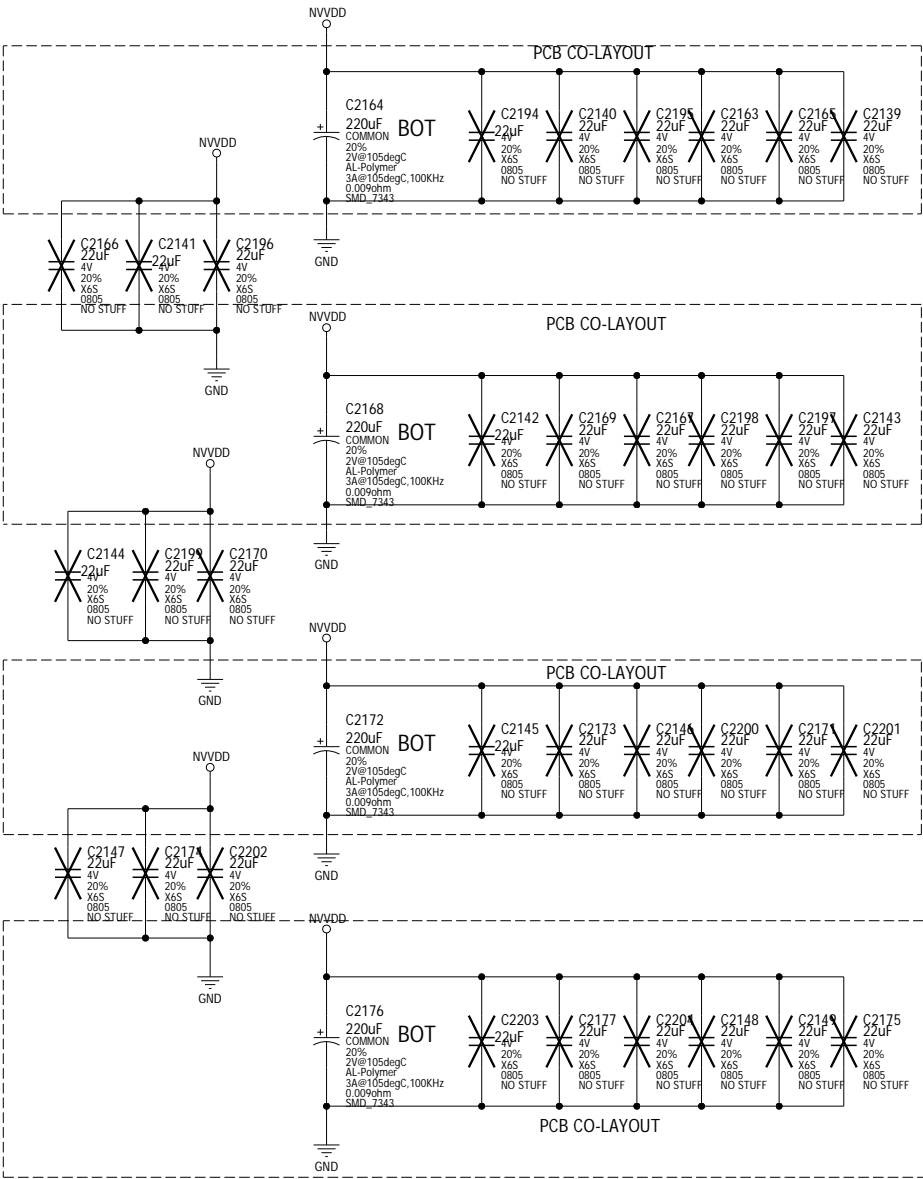
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NV_PN	600-1G136-0010-300
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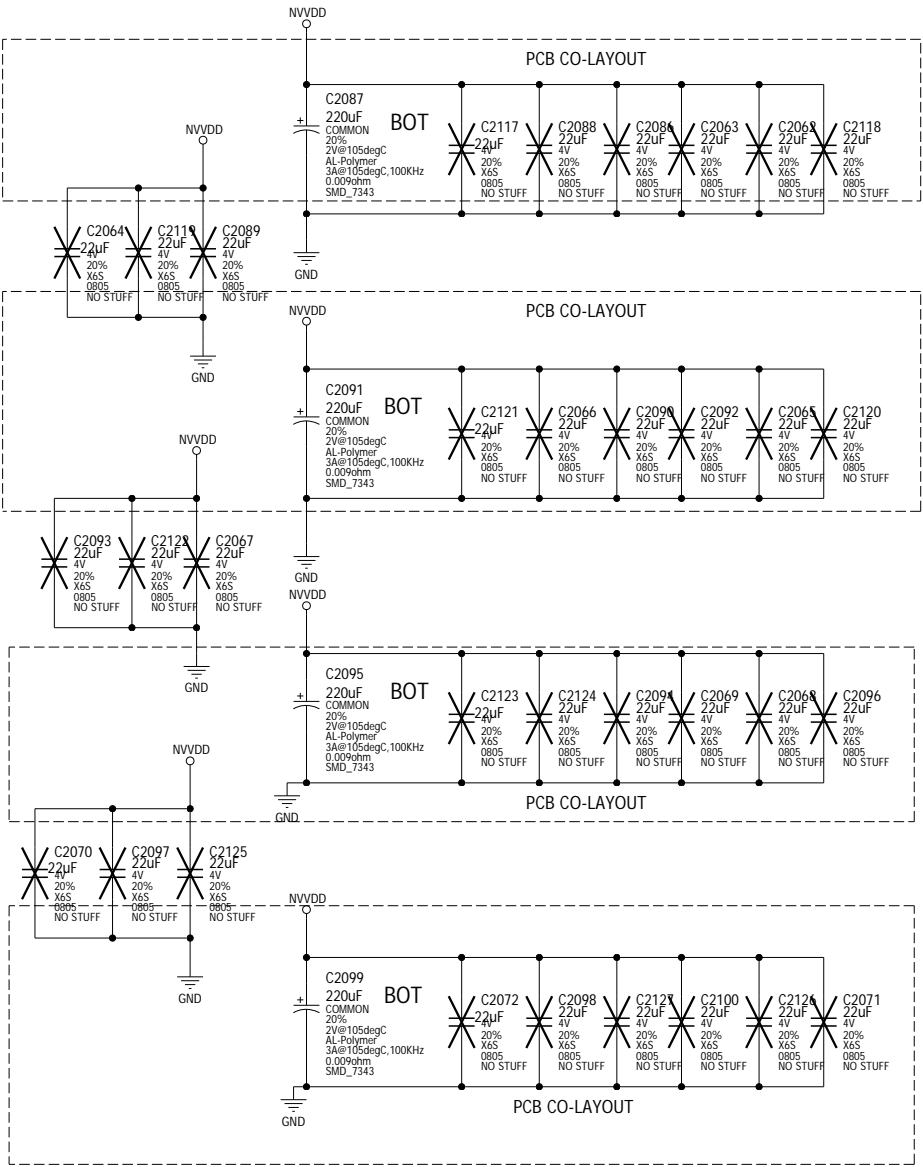
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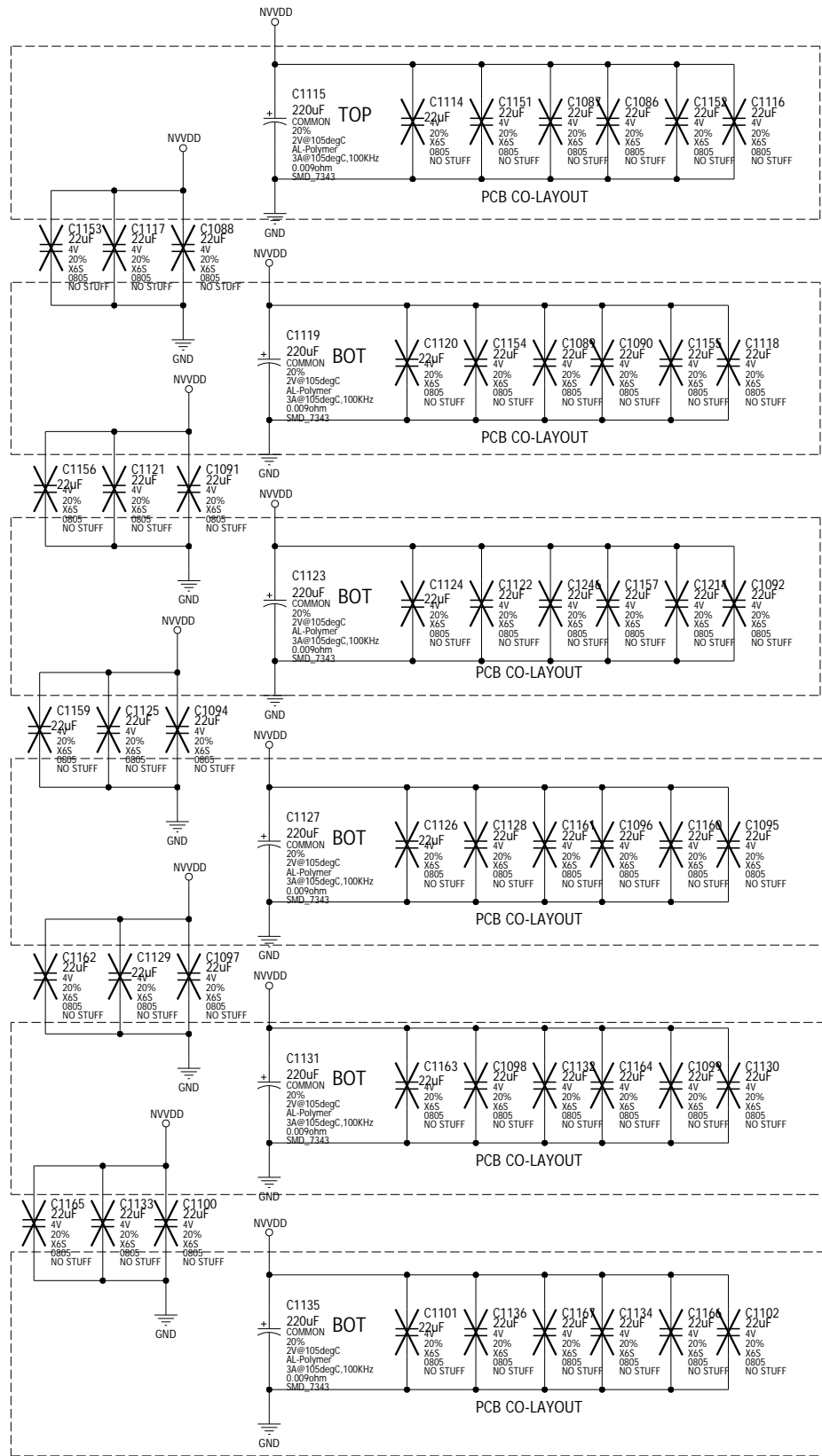
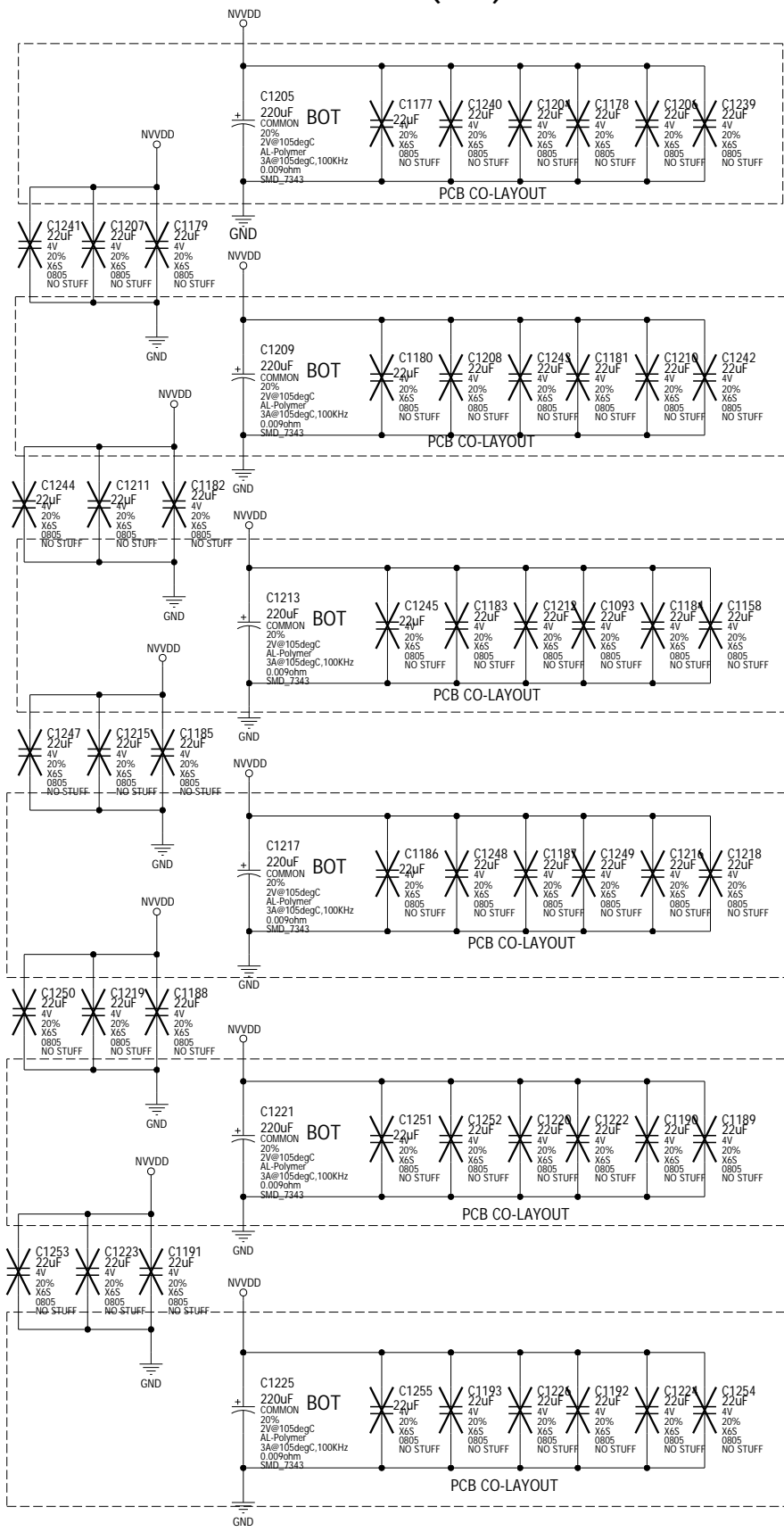
20x SMD7343 330uF CO-LAYOUT WITH 120x 0805 22uF



BACK WEST OF PCB

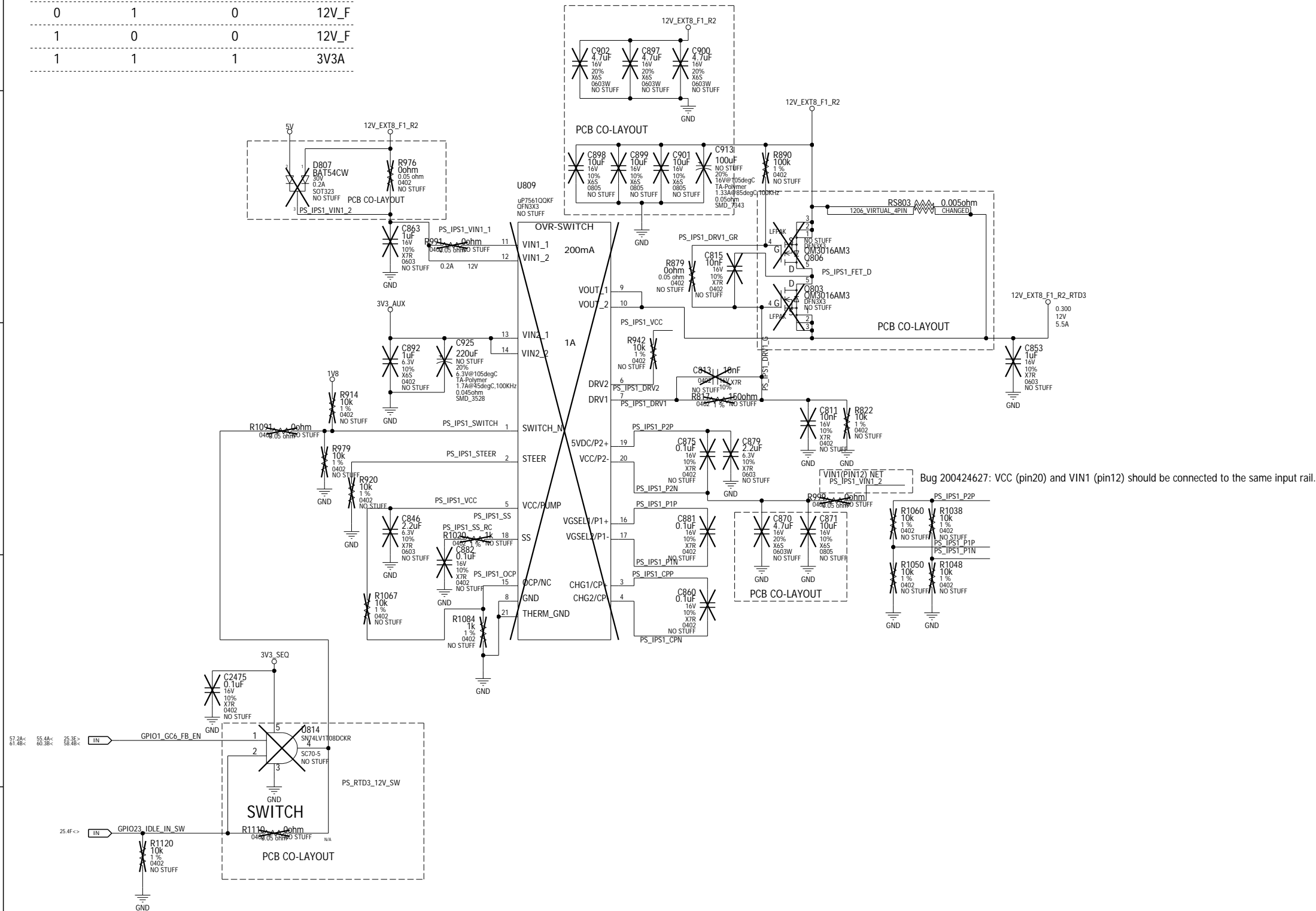


BACK WEST OF PCB

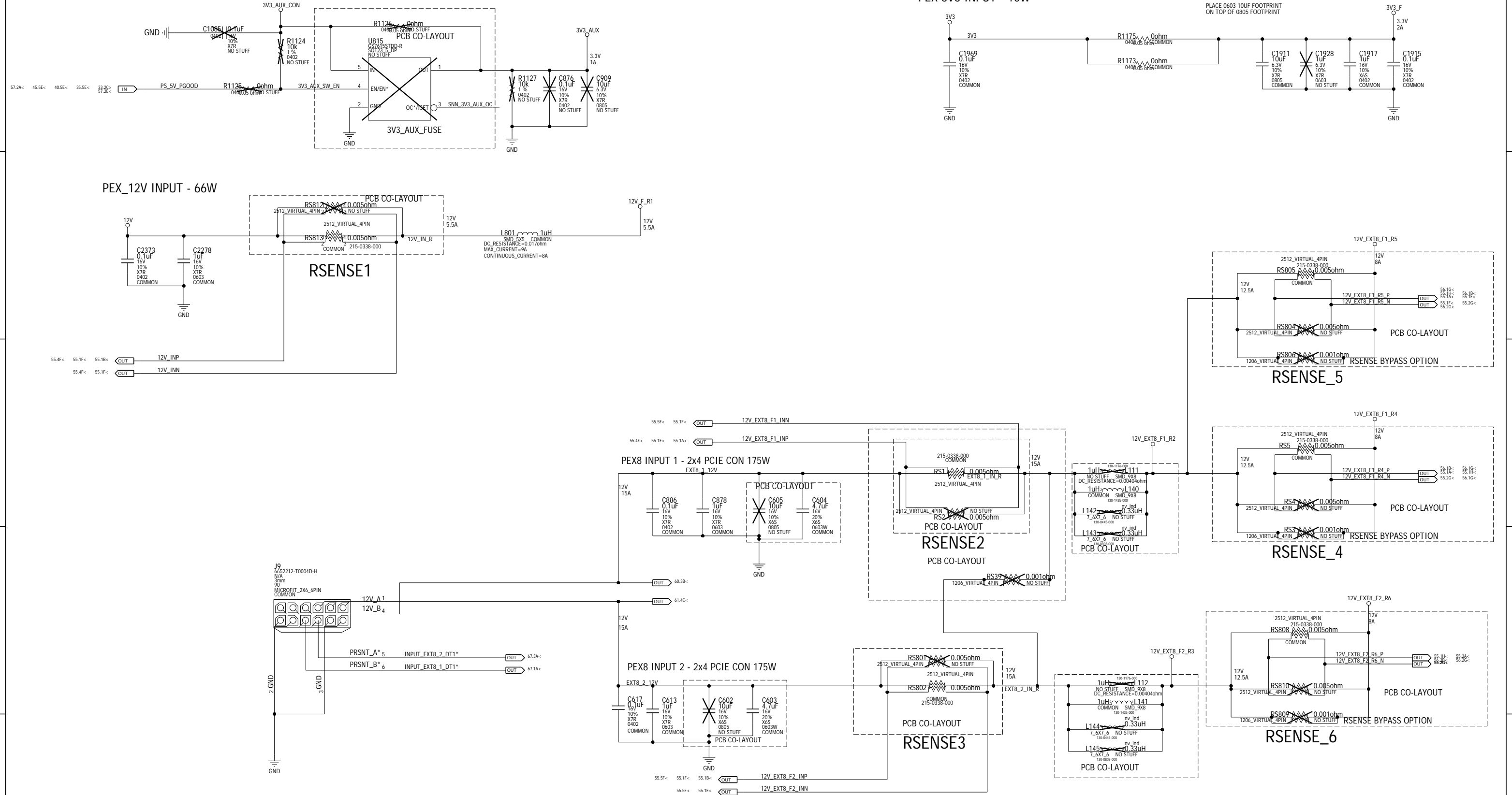


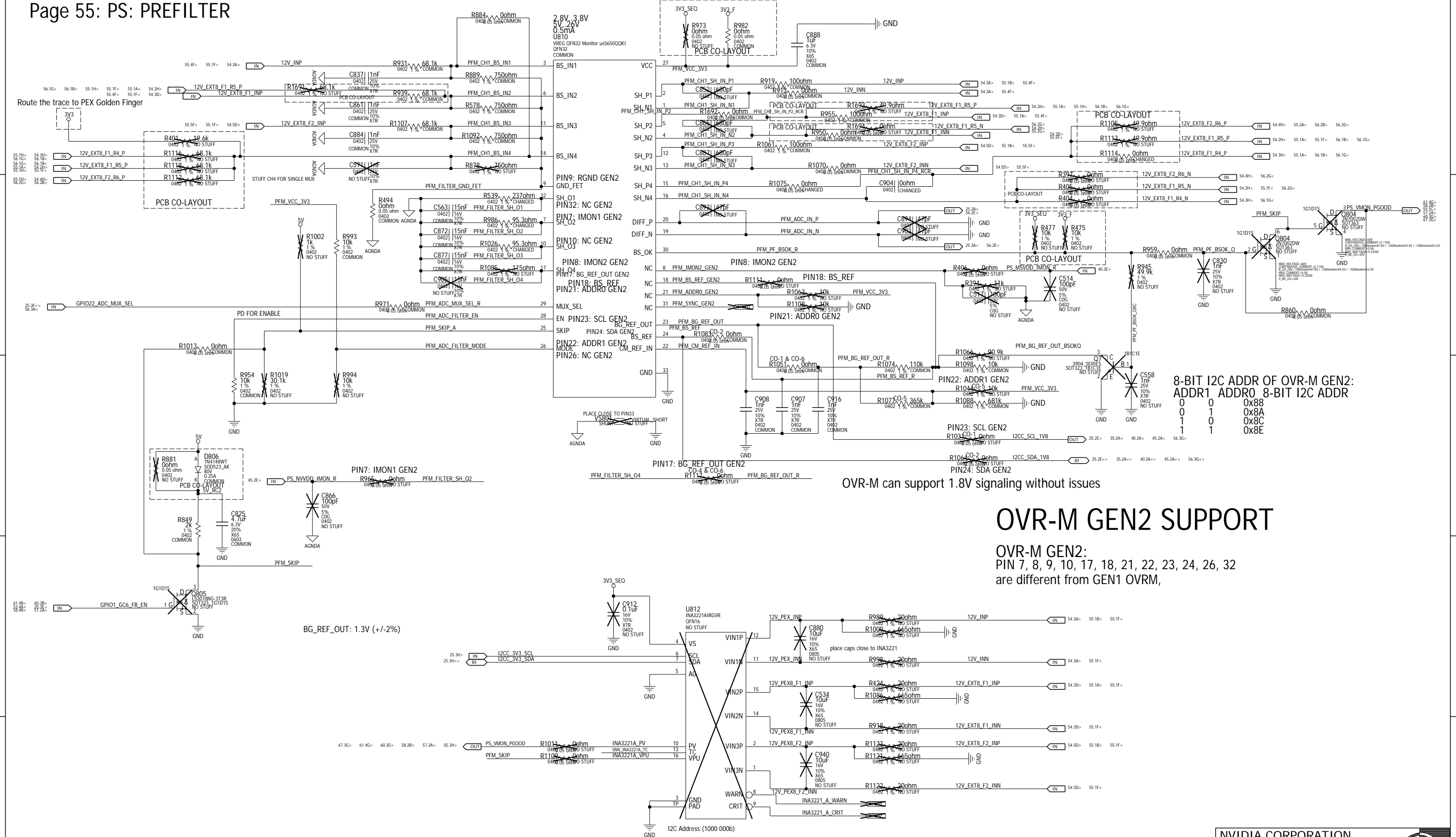
AND GATE LOGIC FOR P-BOARD

GPI01	GPI029	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

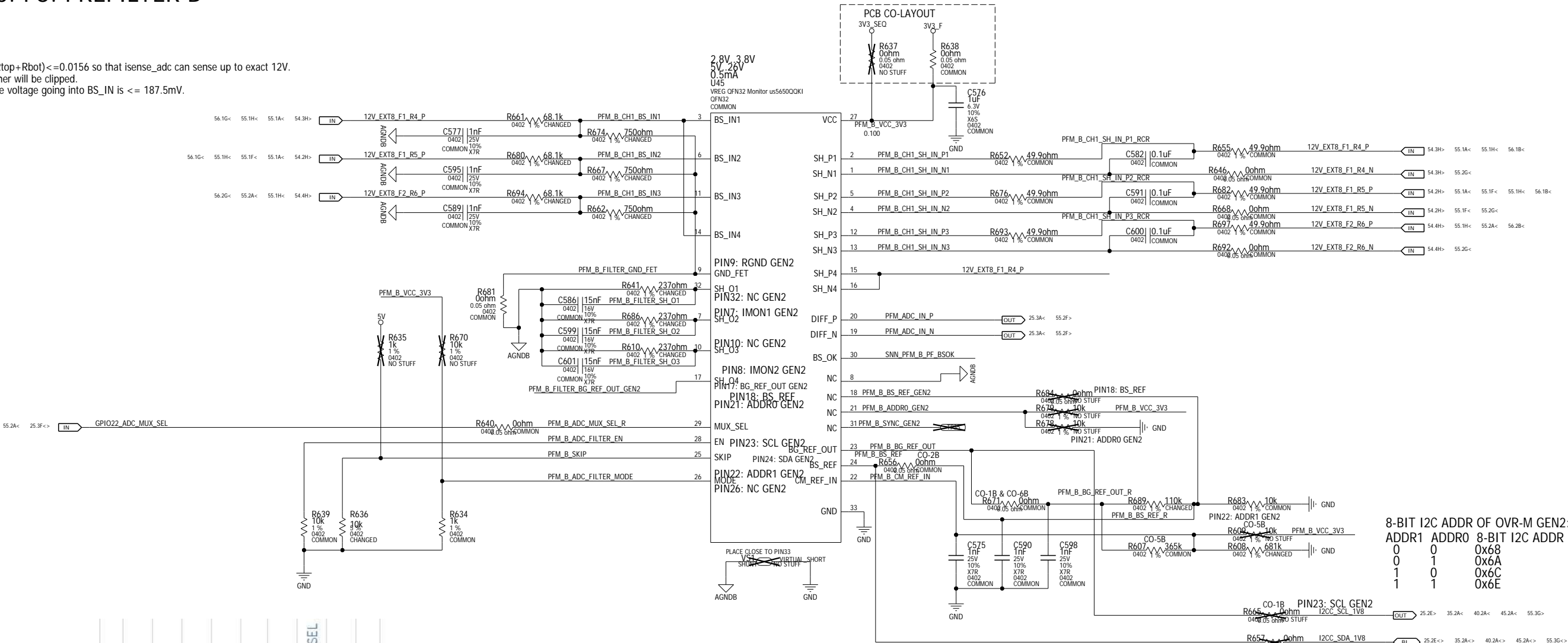


Page 54: PS: INPUTS, FILTERING, MONITORING



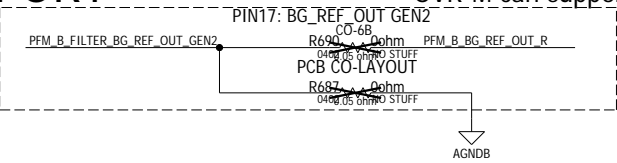


BUS: $R_{bot}/(R_{top}+R_{bot}) \leq 0.0156$ so that `isense_adc` can sense up to exact 12V.
Anything higher will be clipped.
Make sure the voltage going into `BS_IN` is $\leq 187.5mV$.



OVR-M GEN2 SUPPORT

OVR-M can support 1.8V signaling without issues



OVR-M GEN2:

PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32
are different from GEN1 OVRM,

		NC/SH_O1	NC	BS_OK	MUX_SEL	ENABLE	VCC	NC/MODE_SEL	SKIP	
		32	31	30	29	28	27	26	25	
SH_IN_N1	1	33 GND								24 SDA/BS_REF
SH_IN_P1	2									23 SCL/BG_REF_OUT
BS_IN1	3									22 ADDR1/CM_REF_IN
SH_IN_N2	4									21 ADDR0/NC
SH_IN_P2	5									20 DIFF_OUT_P
BS_IN2	6									19 DIFF_OUT_N
IMON1/SH_O2	7									18 BS_REF/NC
IMON2/NC	8									17 BG_REF_OUT/SH_O4
		9	10	11	12	13	14	15	16	
RGND/GND_FET		NC/SH_O3	BS_IN3	SH_IN_P3	SH_IN_N3	BS_IN4	SH_IN_P4	SH_IN_N4		

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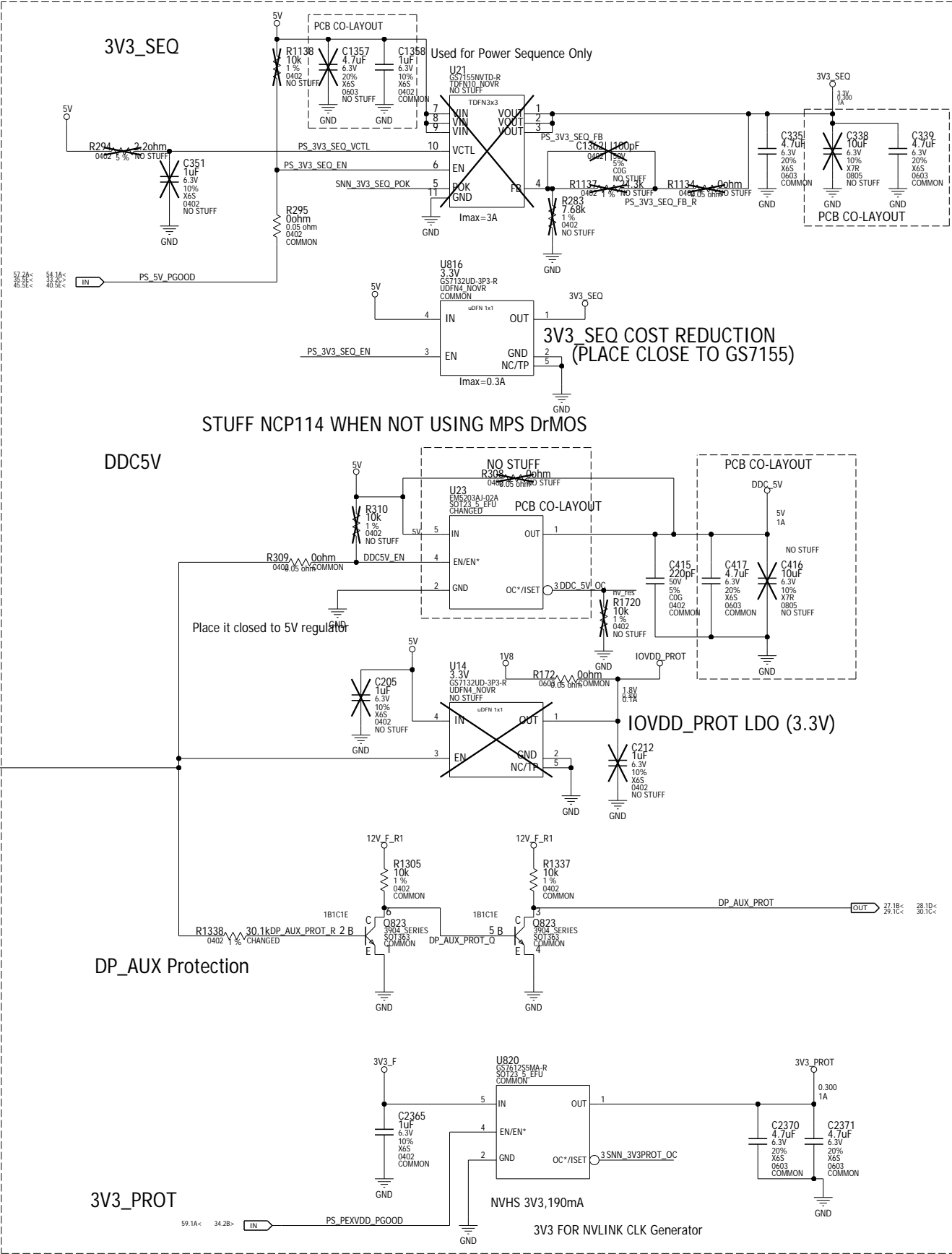
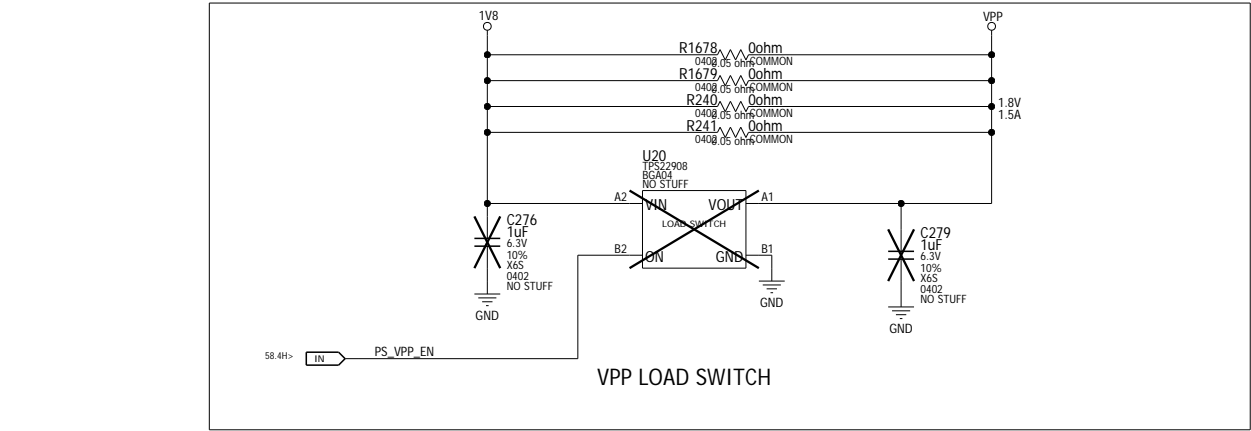
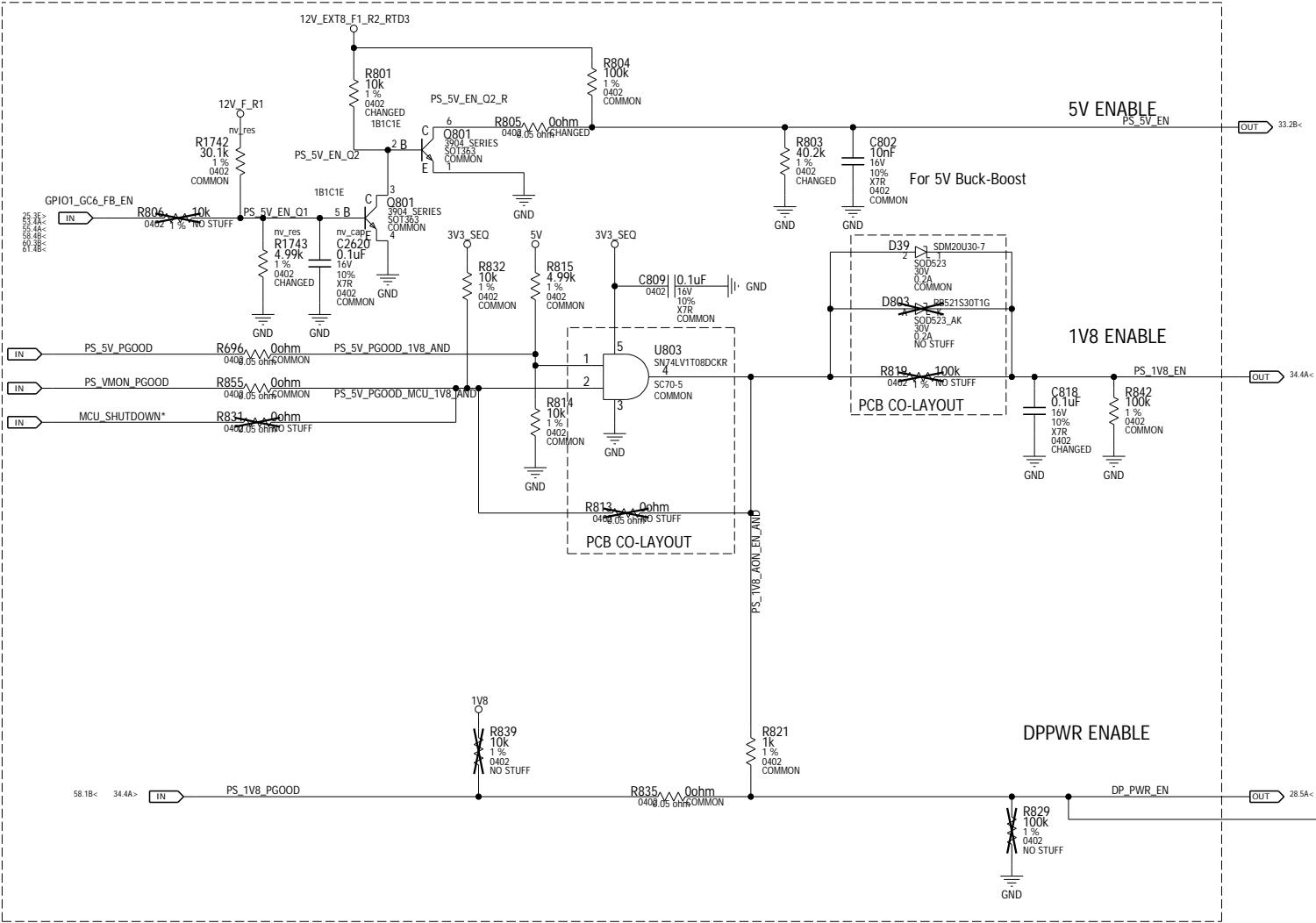


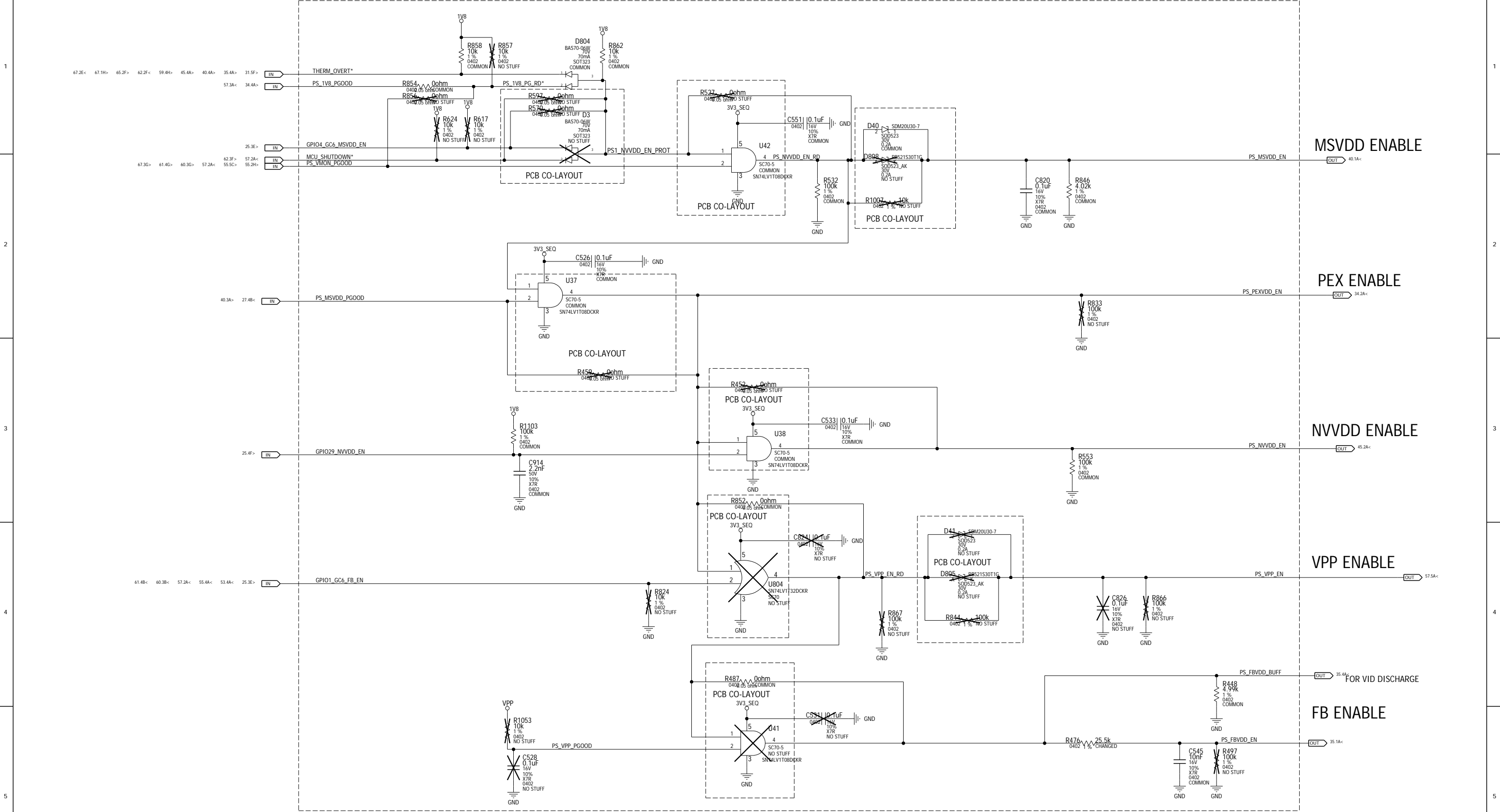
NV_PN 600-1G136-0010-300

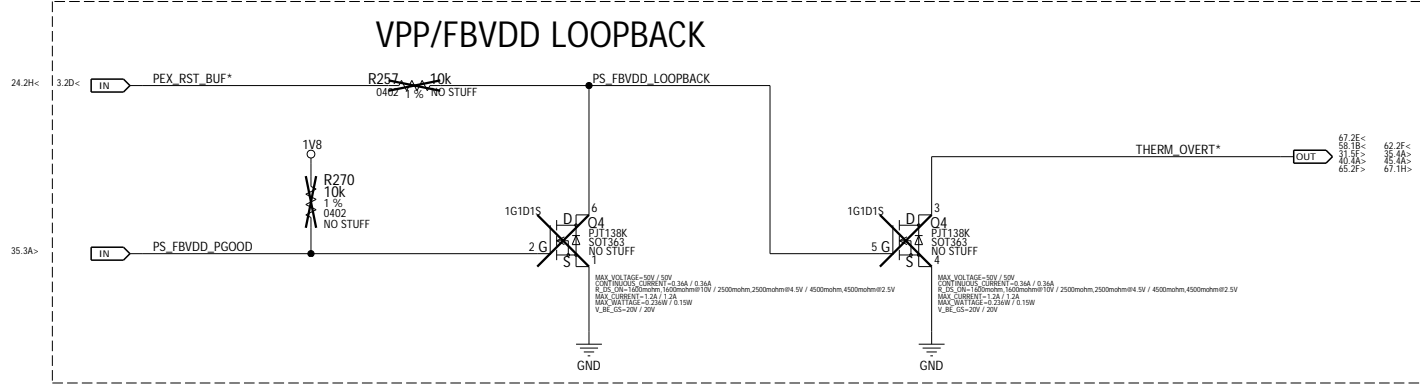
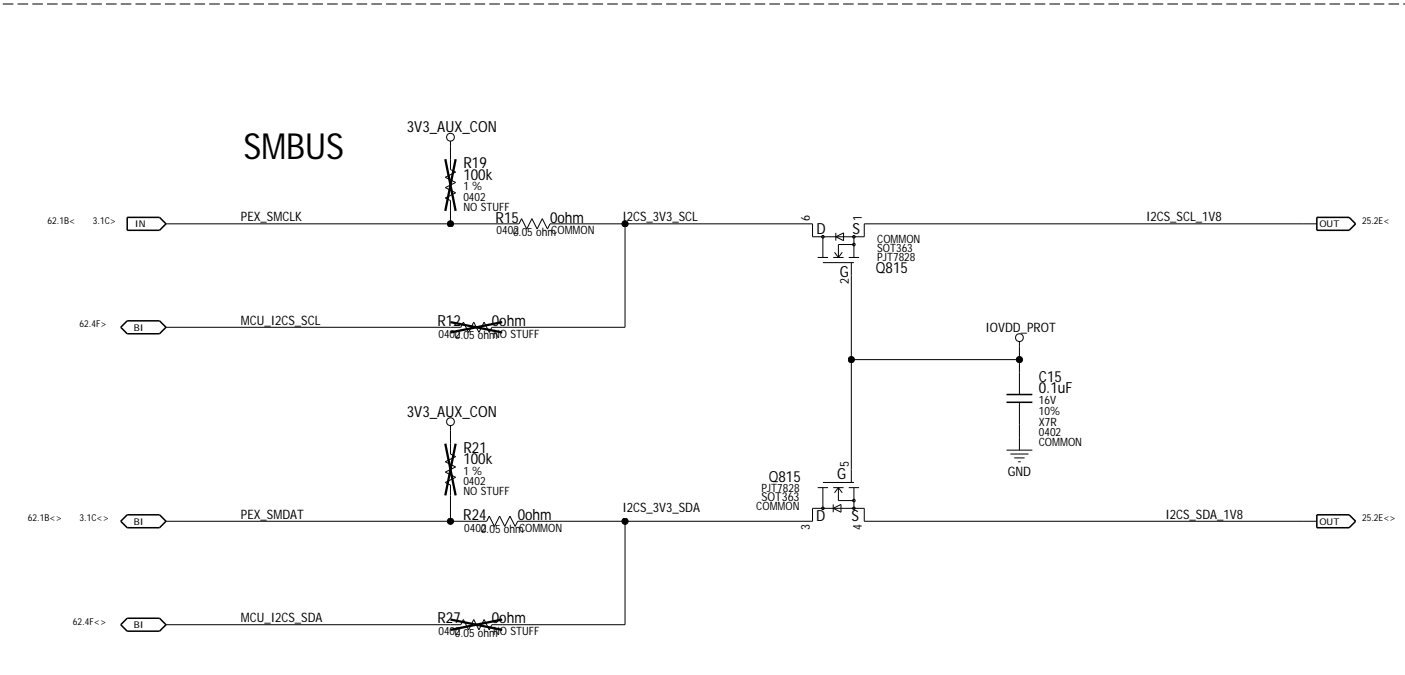
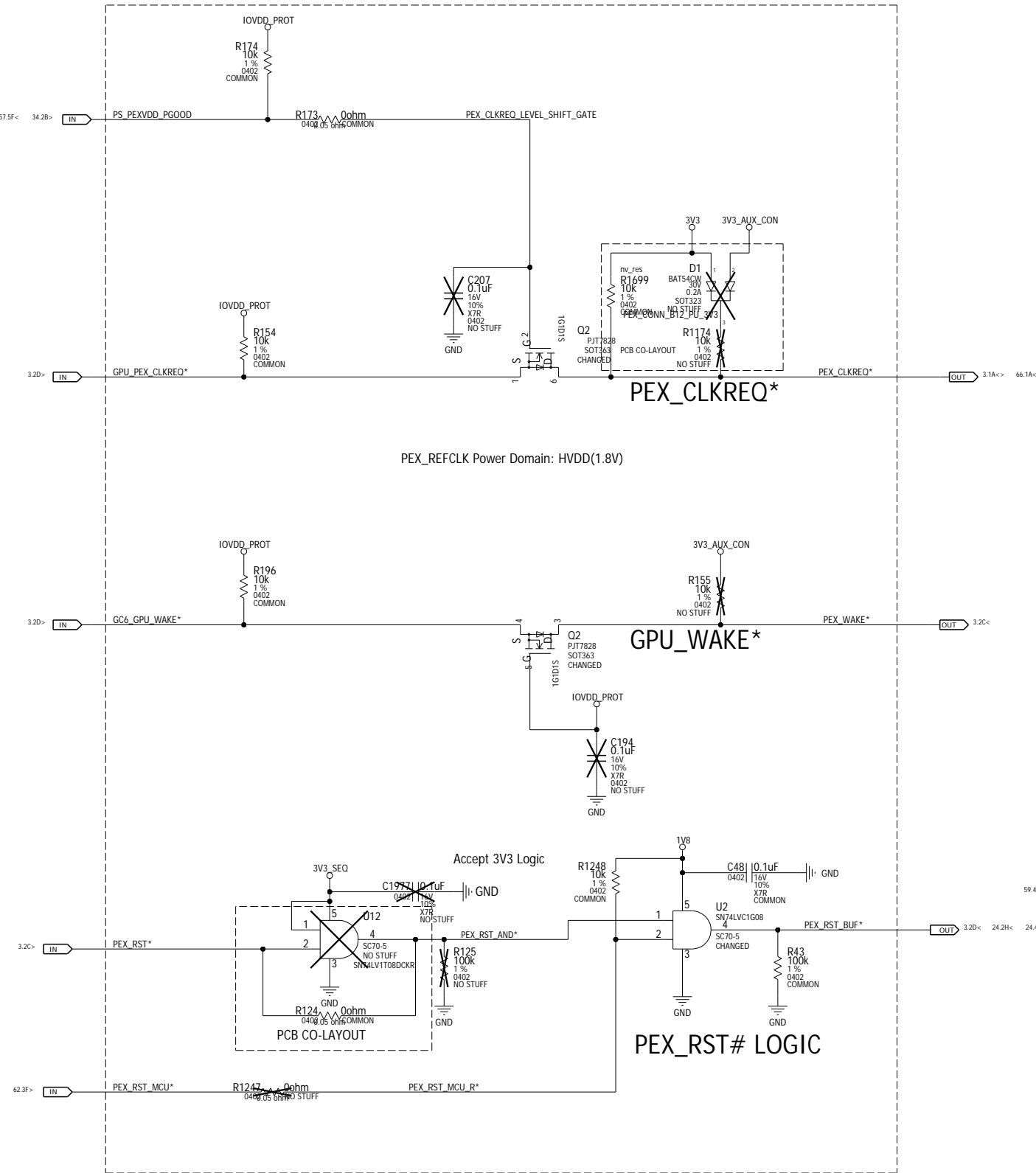
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: PREFILTER B

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1.5%). $V_{\text{hys}}(\text{Typ})=0.01 \cdot V_{\text{th}}$, $V_{\text{hys}}(\text{Max})=0.016 \cdot V_{\text{th}}$

- 1) Suppose that at $t=0s$, V_{in} is greater than $(2.7V + V_{hys})$, $V_{reset}=LOW$. After V_{in} decreases to $2.7V (+/- 0.0405V)$, $V_{reset}=floating$.
- 2) Suppose that at $t=0s$, V_{in} is smaller than $(2.7V)$, $V_{reset}=floating$. After V_{in} increases to $[2.7V (+/- 0.0405V) + V_{hys}]$, $V_{reset}=LOW$.

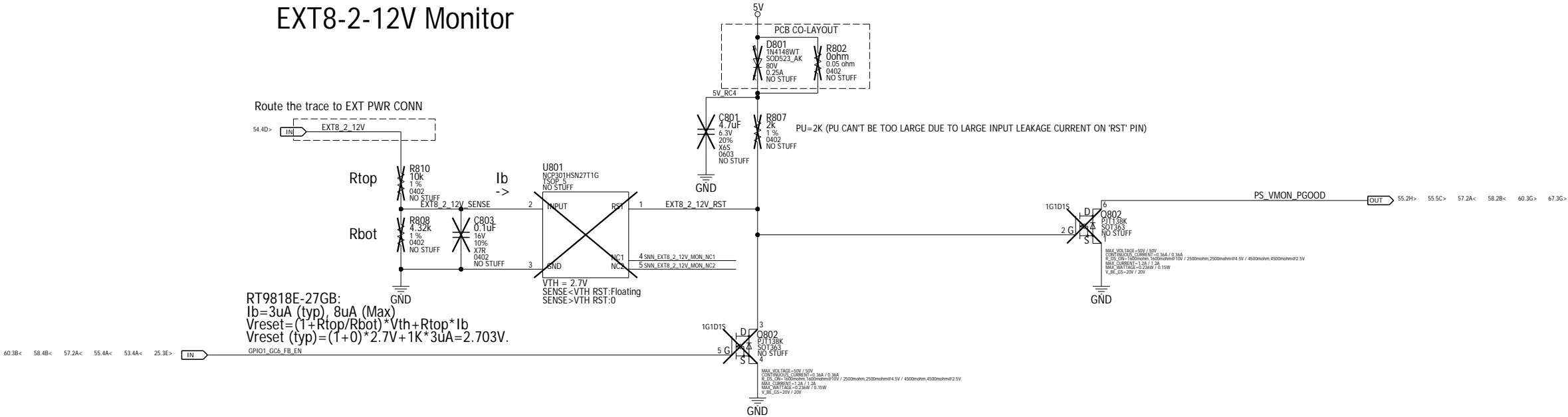


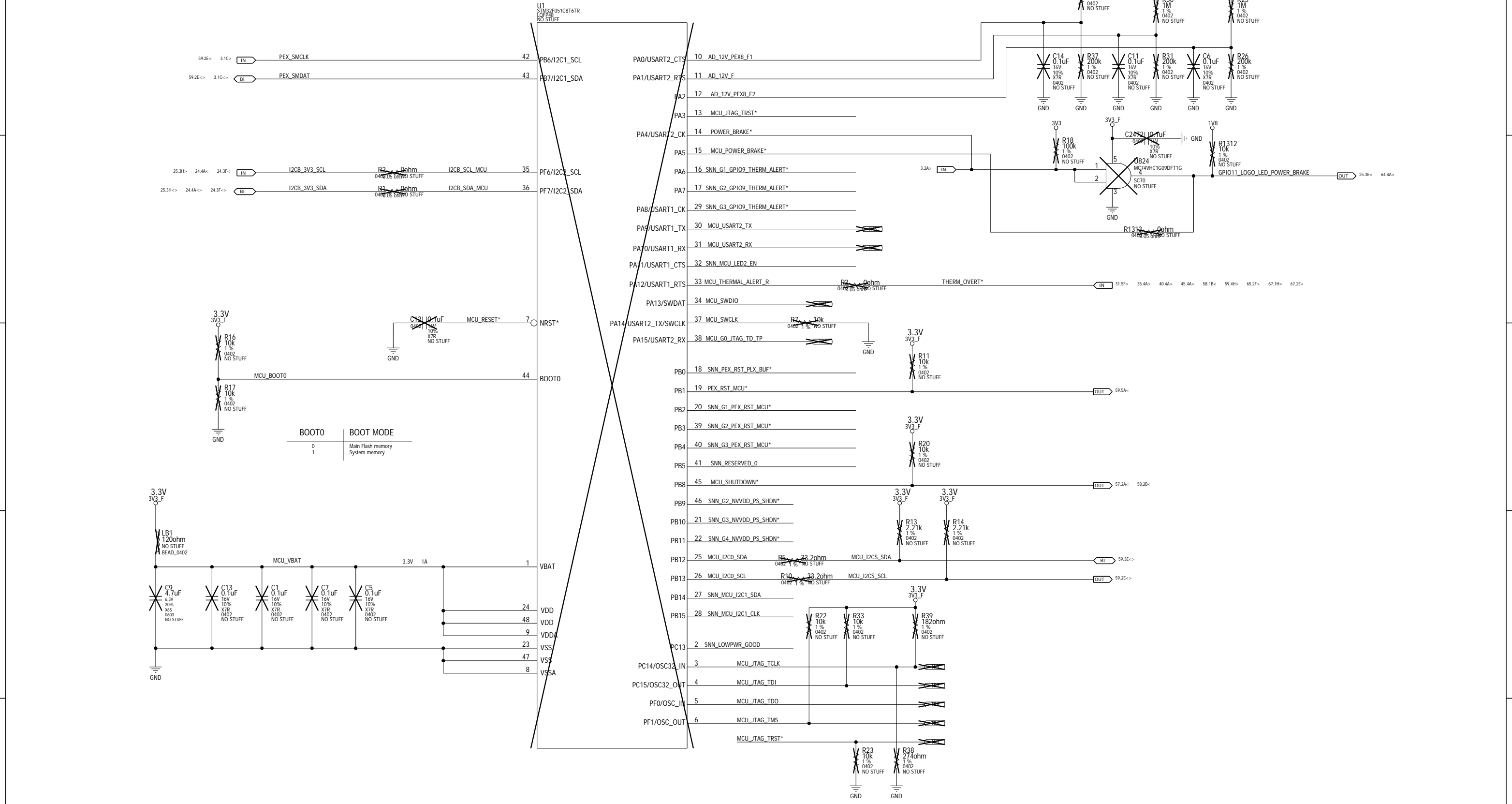
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_CN 600-1G136-0010-300				
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BOM REV	B	DATE	26-JUN-2020	

H

EXT8-1-12V Monitor: Co-layout with PEX3V3 Monitor

EXT8-2-12V Monitor

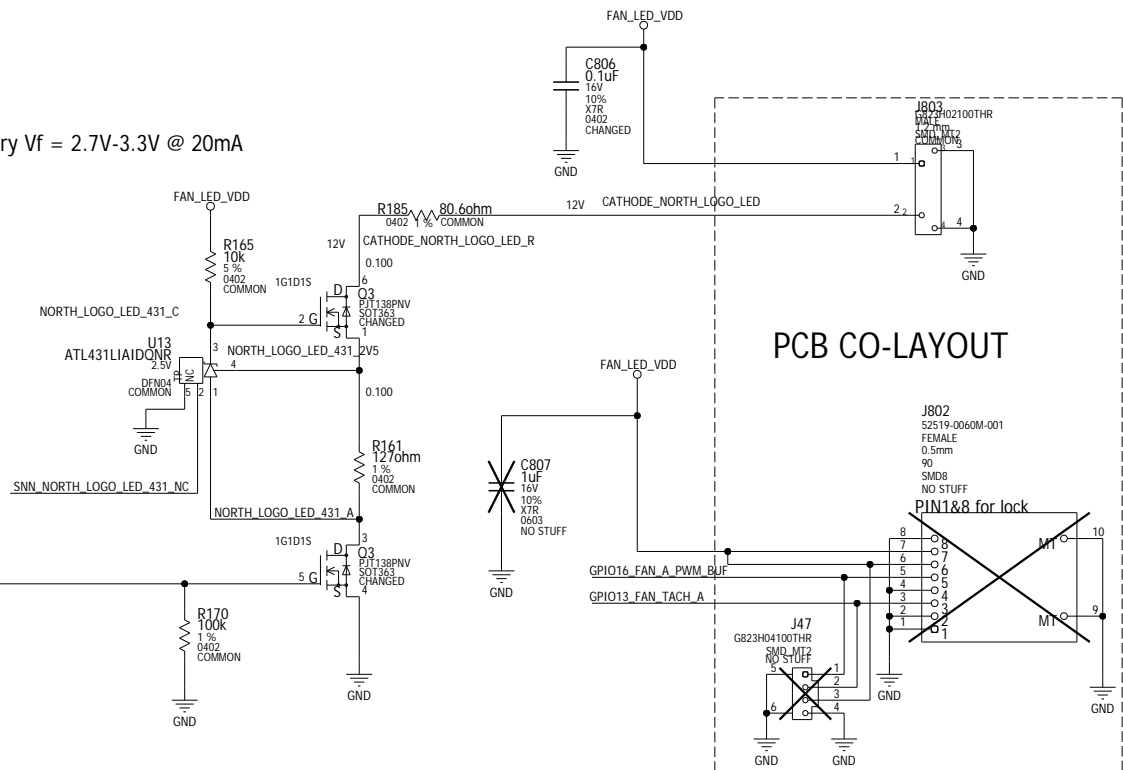




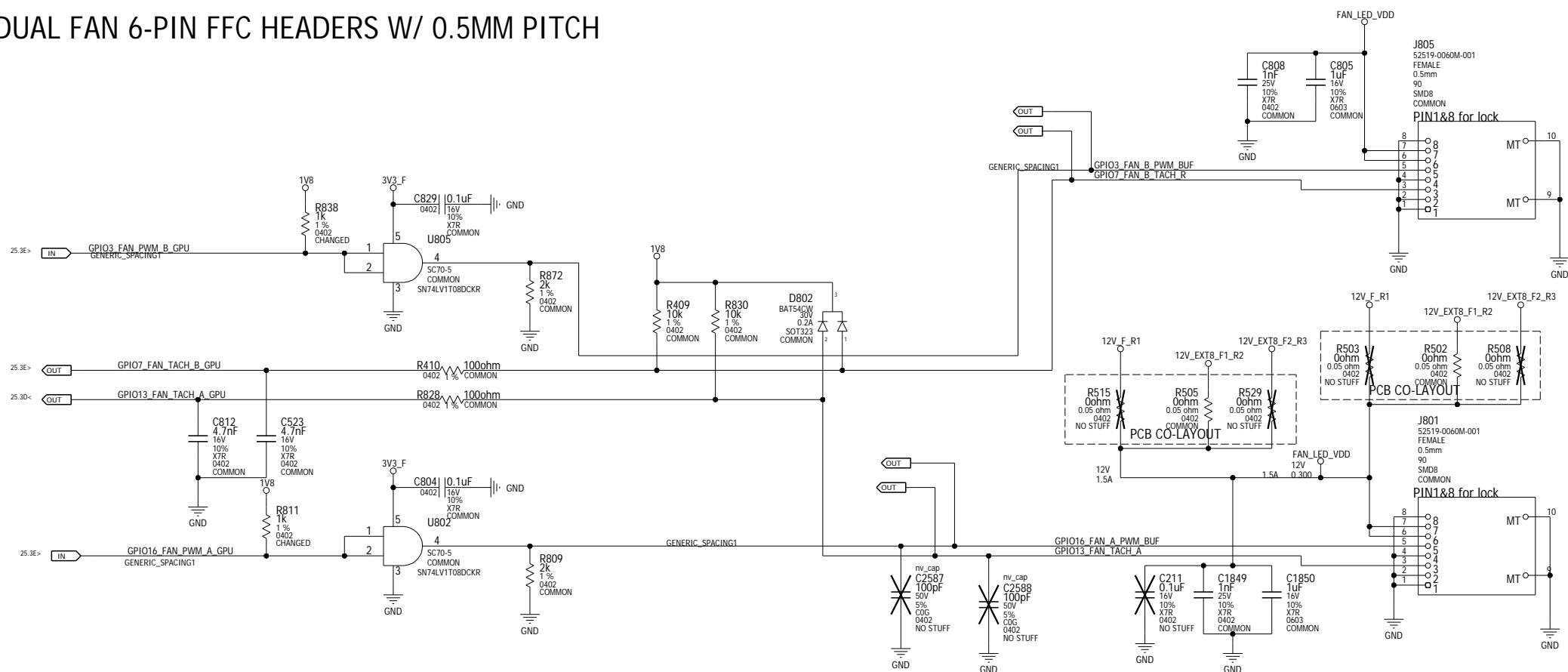
White LED: Preliminary $V_f = 2.7V-3.3V @ 20mA$

(LED should not blink during boot)

NOTE: LED POR IS NOT SET YET.



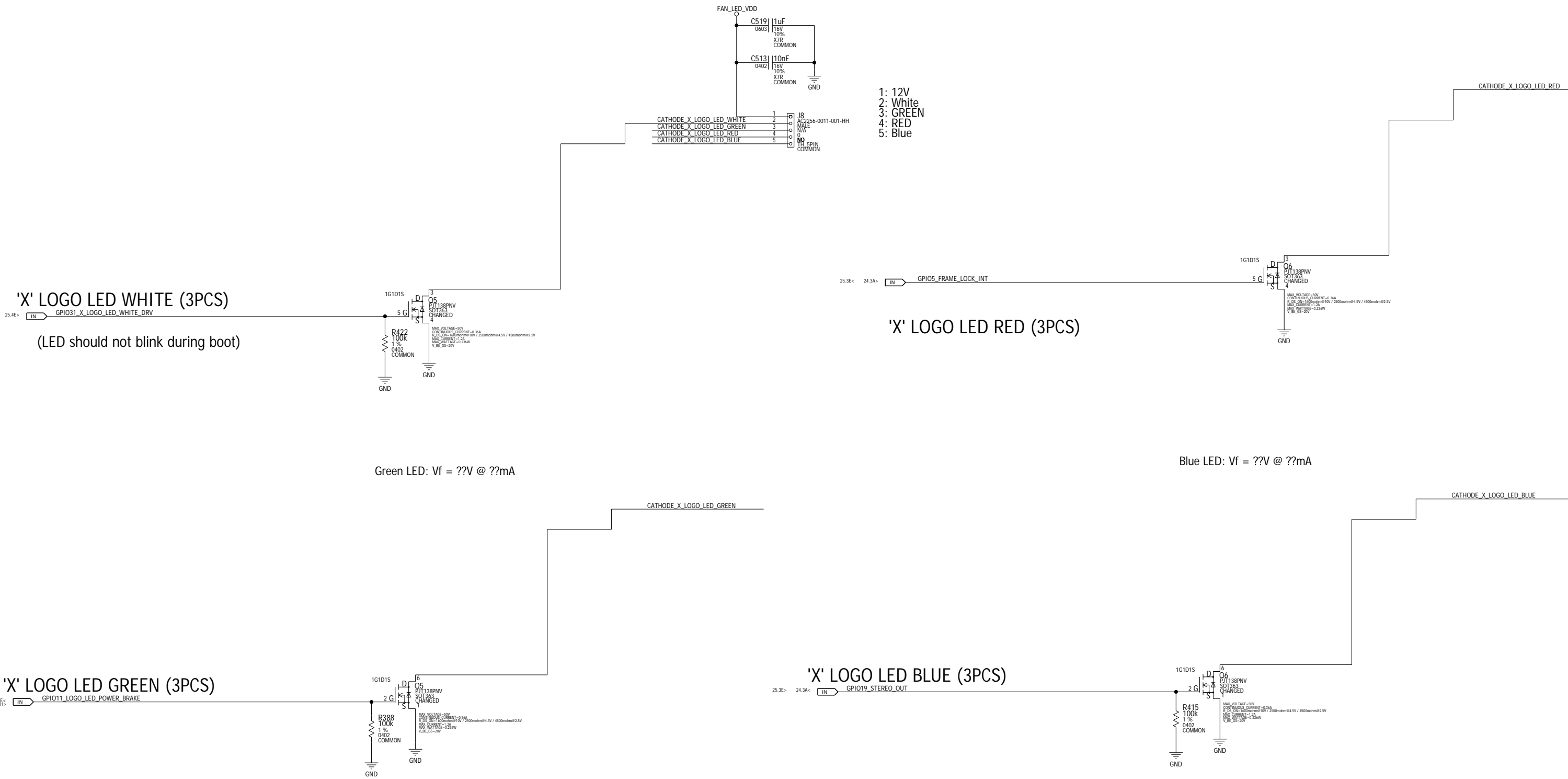
FAN A (LEFT)

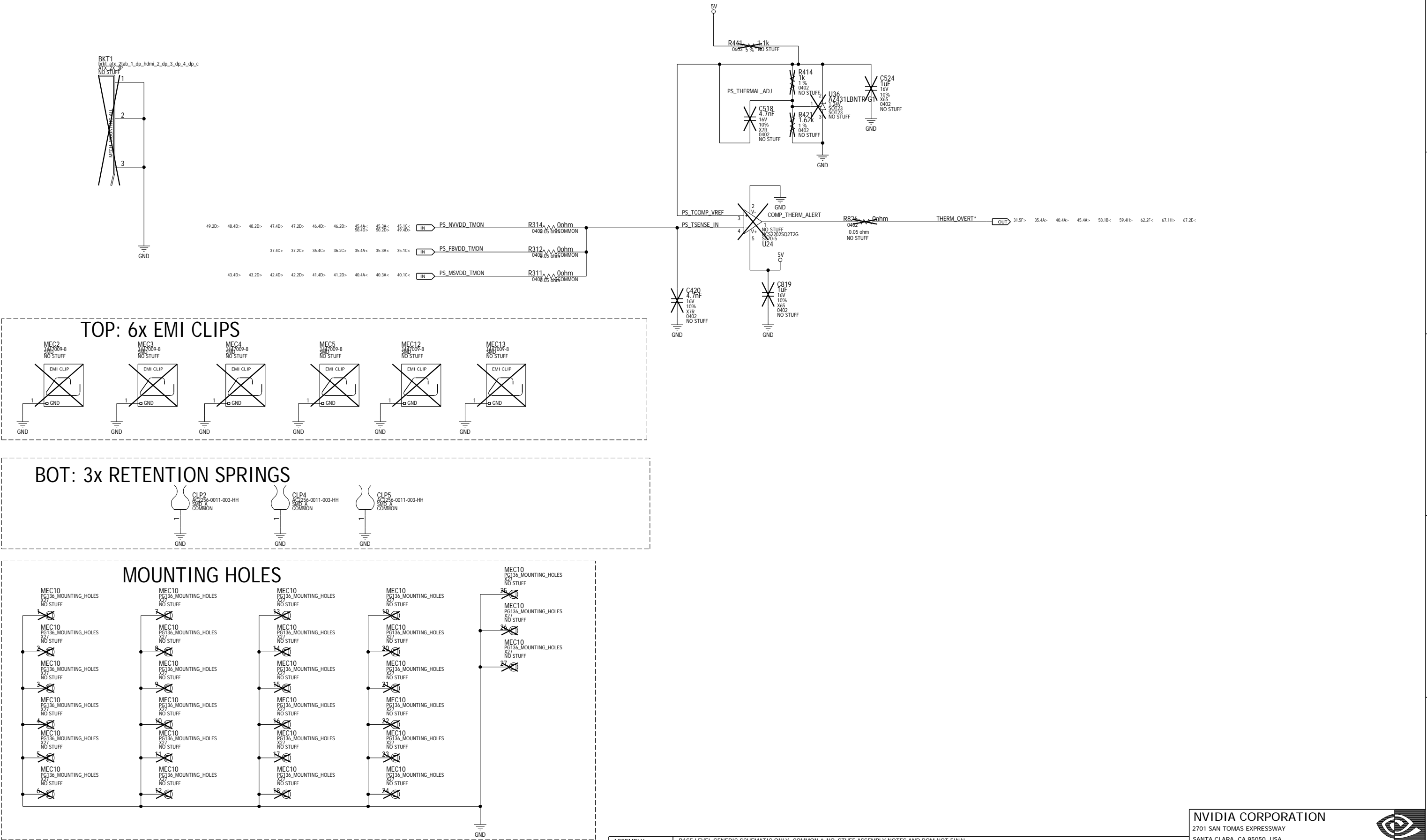


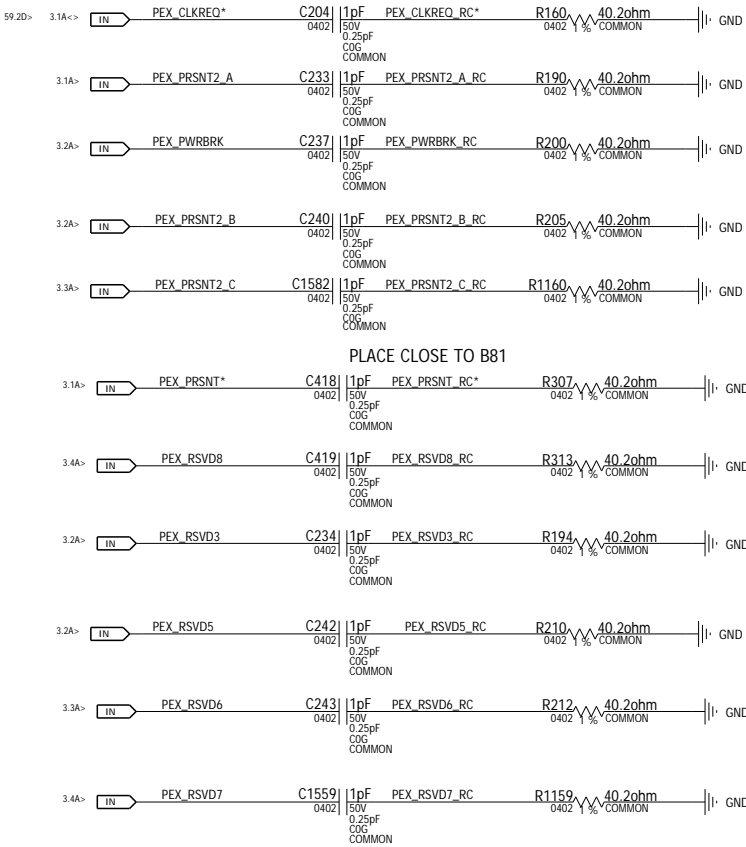
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NOTE: LED POR IS NOT SET YET.

5-PIN POGO-PIN HEADERS FOR 'X' LOGO LEDs







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